

# EBSA-110 Schematic Directory

BAN# = EBSA-110 - STRONGARM EVALUATION BOARD  
REV# = REV B

SHEET	SIG PREFIXES	DESCRIPTION
sht 1	-	Schematic Directory
sht 2	-	Block diagram
sht 3	CPU_, ECH_, 3V3_	CPU, clock, level-shifting
sht 4	-	Debug pick-up points
sht 5	-	SSRAM
sht 6	BUF_, IO_	Address and data buffering
sht 7	MUX_, SIM_	DRAM address MUXing and SIMMs
sht 8	CTA_, CTB_	Control state machines
sht 9	CTA_, CTB_	Series terminations and decoupling for sht8
sht 10	ROM_	EPROM/Flash with byte->word packer
sht 11	SUP_, CON_	Super I/O
sht 12	MAX_, IND_, CON_	Super I/O RS232 drivers and connectors
sht 13	NET_	Ethernet controller with clock & LEDs
sht 14	-	Ethernet buffer RAM and address ROM
sht 15	-	Ethernet media interface
sht 16	CIA_	PCMCIA controller
sht 17	PWA_, PWB_, SLA_, SLB_	PCMCIA connector and power control
sht 18	TAG_, RST_, BUF_	JTAG connector & buffers, reset circuitry
sht 19	PIT_, SPR_	Timer (PIT), spare gates, CPU decoupling
sht 20	-	Power regulation
sht 21	-	Power connectors and bulk decoupling
sht 22	LNK_, ANA_	Configuration jumpers

Note:  
CTB\_DBG (SHT 8)  
has no fanout

## JUMPERS

SHT20, SHT22

## PICKUPS

SHT4, SHT20

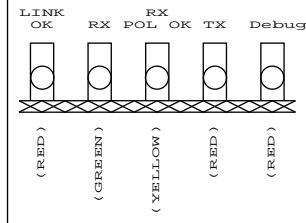
## CONNECTORS

SHT12, SHT15, SHT17  
SHT18, SHT21

## LINKS

SHT3, SHT5, SHT19

## LEDs



- All signals have a 3-letter prefix of their origin  
(for bidirects this is the arbitrarily Most Important Driver)
- Side-2 Etchlinks start at EL101
- Side-2 capacitors start at C301
- All other components are on side 1

2-13-1996\_18:33

REVISION		
CHK	CHANGE NO.	REV

<b>digital</b>	DRN.	DATE
CHK'D.	DATE	REV.
EBSA#	EBSA#	EBSA#
PART# USED ON OPTION/MODEL	POP DOCUMENT NUMBER	POP DOCUMENT NUMBER

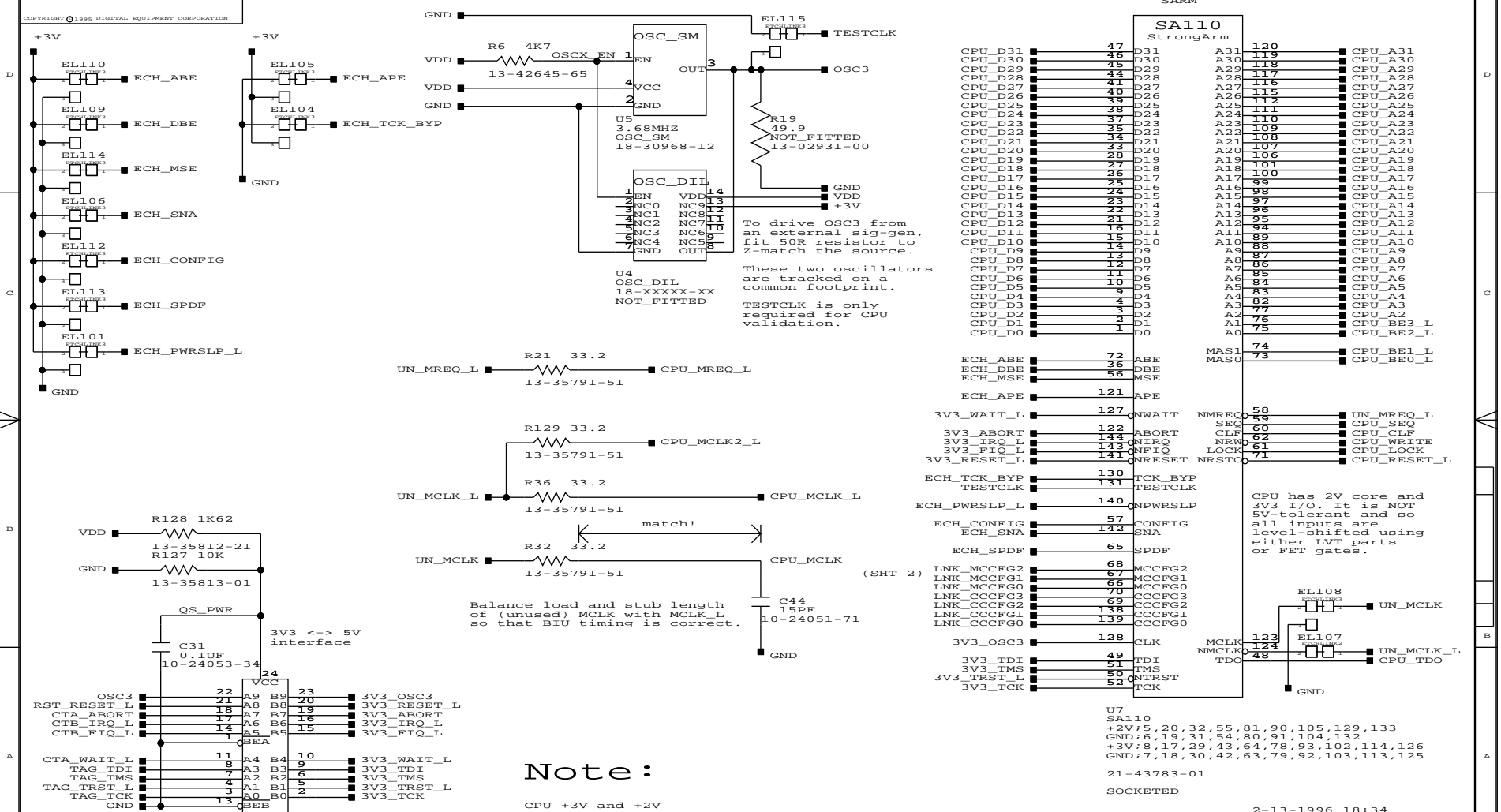
N. Crook	DATE
BOARD LOCATION	DATE
SHEET	DATE
POP DOCUMENT NUMBER	DATE

TITLE			
ebsa110 1			
SIZE	CODE	NUMBER	REV.
B			



# CPU, clock, level shift & decouplers

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SARM

SA110 StrongArm	
CPU_D31	47 D31
CPU_D30	46 D30
CPU_D29	45 D29
CPU_D28	44 D28
CPU_D27	41 D27
CPU_D26	40 D26
CPU_D25	39 D25
CPU_D24	38 D24
CPU_D23	37 D23
CPU_D22	35 D22
CPU_D21	34 D21
CPU_D20	33 D20
CPU_D19	28 D19
CPU_D18	26 D18
CPU_D17	27 D17
CPU_D16	25 D16
CPU_D15	23 D15
CPU_D14	22 D14
CPU_D13	21 D13
CPU_D12	21 D12
CPU_D11	15 D11
CPU_D10	14 D10
CPU_D9	14 D9
CPU_D8	12 D8
CPU_D7	11 D7
CPU_D6	10 D6
CPU_D5	10 D5
CPU_D4	4 D4
CPU_D3	3 D3
CPU_D2	3 D2
CPU_D1	2 D1
CPU_D0	1 D0
A31	120 CPU_A31
A30	119 CPU_A30
A29	117 CPU_A29
A28	117 CPU_A28
A27	116 CPU_A27
A26	112 CPU_A26
A25	111 CPU_A25
A24	109 CPU_A24
A23	110 CPU_A23
A22	108 CPU_A22
A21	101 CPU_A21
A20	107 CPU_A20
A19	106 CPU_A19
A18	101 CPU_A18
A17	101 CPU_A17
A16	99 CPU_A16
A15	98 CPU_A15
A14	96 CPU_A14
A13	96 CPU_A13
A12	94 CPU_A12
A11	89 CPU_A11
A10	87 CPU_A10
A9	88 CPU_A9
A8	86 CPU_A8
A7	85 CPU_A7
A6	84 CPU_A6
A5	83 CPU_A5
A4	82 CPU_A4
A3	77 CPU_A3
A2	77 CPU_A2
A1	76 CPU_BE3_L
A0	75 CPU_BE2_L
MAS1	74 CPU_BE1_L
MAS0	73 CPU_BE0_L
ABE	72 ABE
DDBE	36 DDBE
MSE	56 MSE
APE	121 APE
NMREQ	58 UN_MREQ_L
SEC	59 CPU_SEC
CLF	60 CPU_CLF
NRW	62 CPU_WRITE
LOCK	61 CPU_LOCK
NRSTO	71 CPU_RESET_L
UN_MREQ_L	58 UN_MREQ_L
CPU_SEC	59 CPU_SEC
CPU_CLF	60 CPU_CLF
CPU_WRITE	62 CPU_WRITE
CPU_LOCK	61 CPU_LOCK
CPU_RESET_L	71 CPU_RESET_L

ECH_ABE	72 ABE
ECH_DBE	36 DDBE
ECH_MSE	56 MSE
UN_MREQ_L	58 UN_MREQ_L
CPU_SEC	59 CPU_SEC
CPU_CLF	60 CPU_CLF
CPU_WRITE	62 CPU_WRITE
CPU_LOCK	61 CPU_LOCK
CPU_RESET_L	71 CPU_RESET_L

ECH_APE	121 APE
3V3_WAIT_L	127 UNWAIT
3V3_ABORT	122 ABORT
3V3_IRQ_L	143 NIRO
3V3_FIQ_L	143 CNFIQ
3V3_RESET_L	141 CNRESET
ECH_TCK_BYP	130 TCK_BYP
TESTCLK	131 TESTCLK
ECH_PWRSLP_L	140 CNPWRSLP
ECH_CONFIG	57 CONFIG
ECH_SNA	142 SNA
ECH_SPDF	65 SPDF
LNK_MCCFG2	68 MCCFG2
LNK_MCCFG1	67 MCCFG1
LNK_MCCFG0	66 MCCFG0
LNK_CCCFG3	70 CCCFG3
LNK_CCCFG2	69 CCCFG2
LNK_CCCFG1	138 CCCFG1
LNK_CCCFG0	139 CCCFG0
3V3_OSC3	128 CLK
3V3_TDI	49 TDI
3V3_TMS	51 TMS
3V3_TRST_L	50 NTRST
3V3_TCK	52 TCK
MCLK	123 MCLK
NMCLK	124 NMCLK
TDO	48 TDO

CPU has 2V core and 3V3 I/O. It is NOT 5V-tolerant and so all inputs are level-shifted using either LVT parts or FET gates.

## Note:

CPU +3V and +2V decoupling is on SHT19

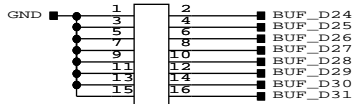
U7 SA110  
 +2V; 5, 20, 32, 55, 81, 90, 105, 129, 133  
 GND; 6, 19, 31, 54, 80, 91, 104, 132  
 +3V; 8, 17, 29, 43, 64, 78, 93, 102, 114, 126  
 GND; 7, 18, 30, 42, 63, 79, 92, 103, 113, 125  
 21-43783-01  
 SOCKETED

2-13-1996_18:34	
DESIGNER: N. Crook	TITLE: ebsa110 3
DATE: _____	OP: _____
TOP DOCUMENT NUMBER: _____	SIZE: B CODE: _____ NUMBER: _____ REV. B

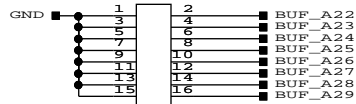
U9 OS3384  
 GND: 12  
 21-40628-02

# CPU pickups

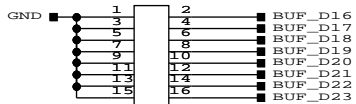
These connectors are pinned to directly connect to a Tektronix DAS logic analyser



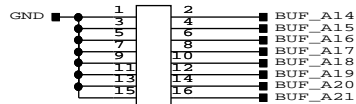
J7 HEAD8X2  
12-13488-13



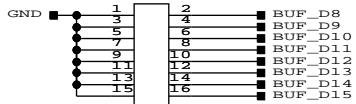
J18 HEAD8X2  
12-13488-13



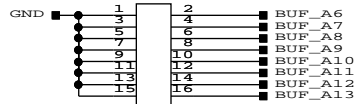
J9 HEAD8X2  
12-13488-13



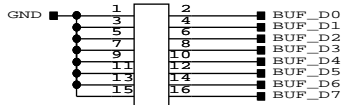
J14 HEAD8X2  
12-13488-13



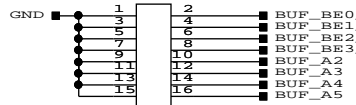
J8 HEAD8X2  
12-13488-13



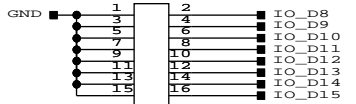
J15 HEAD8X2  
12-13488-13



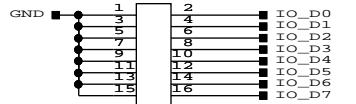
J10 HEAD8X2  
12-13488-13



J16 HEAD8X2  
12-13488-13

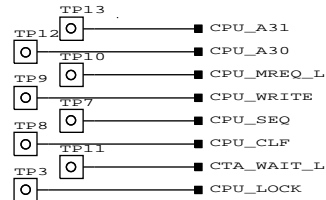


J11 HEAD8X2  
12-13488-13

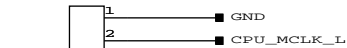


J12 HEAD8X2  
12-13488-13

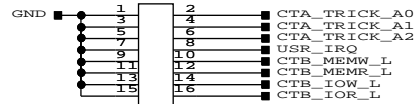
These test points are intended to be big VIAs on the normal daisy-chained etch in order to provide pickup without adding etch length or capacitive load



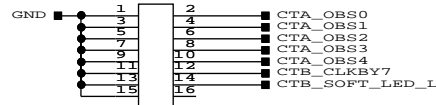
J27 12-15901-05  
NOT\_FITTED



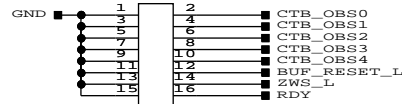
J28 12-15901-05  
NOT\_FITTED



J19 HEAD8X2  
12-13488-13

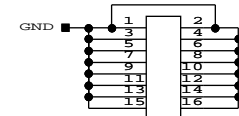


J17 HEAD8X2  
12-13488-13

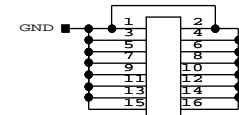


J13 HEAD8X2  
12-13488-13

# OV pickups for DAS



J29 HEAD8X2  
12-13488-13  
NOT\_FITTED



J26 HEAD8X2  
12-13488-13  
NOT\_FITTED

2-13-1996\_18:35

DESIGNER N. Crook	DATE	TITLE ebsa110 4		
WORK LOCATION	OP	SIZE B	CODE	NUMBER
TOP DOCUMENT NUMBER				REV. B

# SSRAM

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This synchronous SRAM has registered outputs

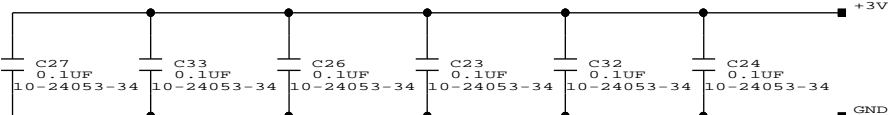
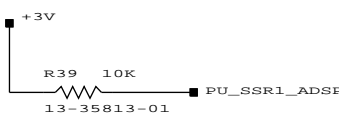
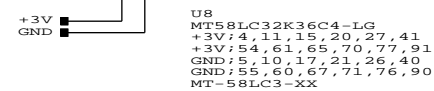
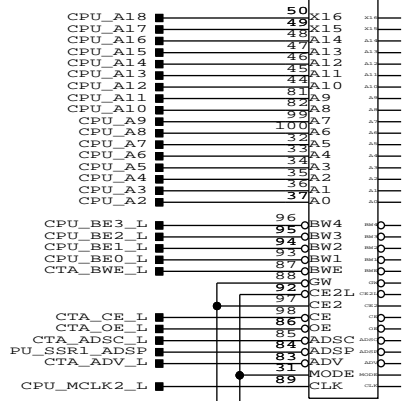
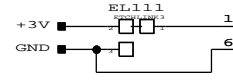
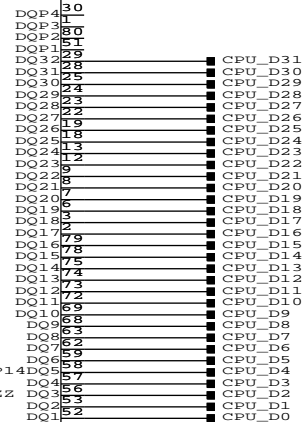
Fit either 32Kx32 or 32Kx36 part

The wiring of pins 14, 64 is intended to accommodate the next-generation parts,

64Kx36. A micron MT58LC64K36C4 or MT58LC64K36D7 should be OK.

## SSRAM36

SS32KX36



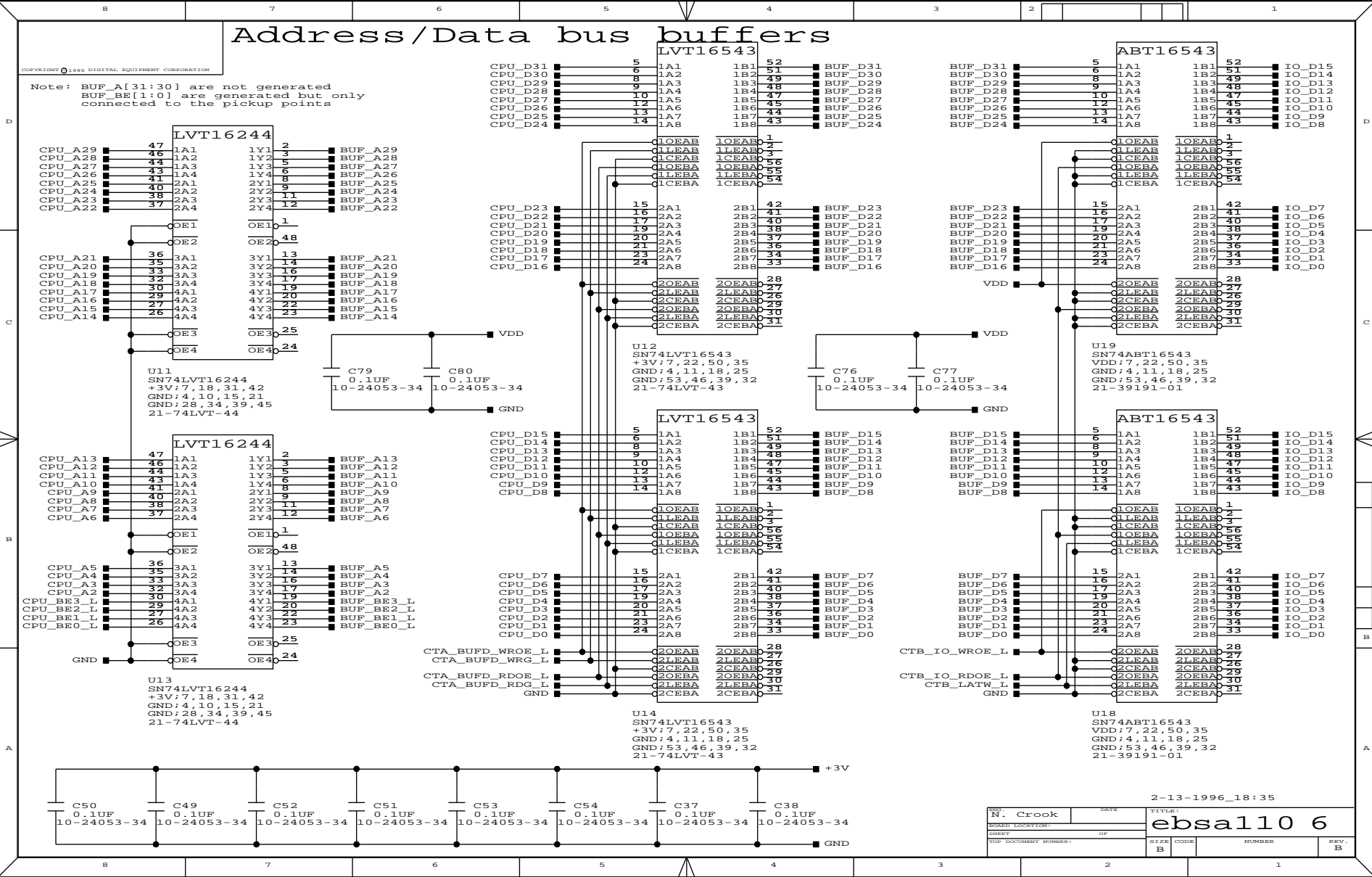
2-13-1996\_18:35

DESIGNER N. Crook	DATE	TITLE <b>esba110 5</b>		
DESIGN LOCATION	OFF	SIZE B	CODE	NUMBER
TOP DOCUMENT NUMBER				REV. B

# Address/Data bus buffers

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Note: BUF\_A[31:30] are not generated  
BUF\_BE[1:0] are generated but only  
connected to the pickup points



2-13-1996\_18:35

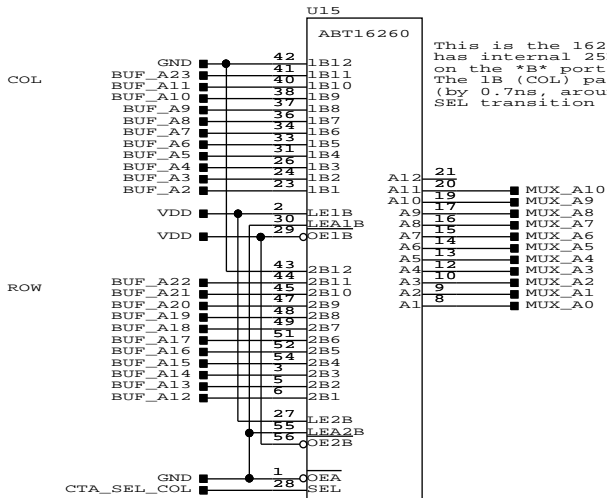
DESIGNER	N. Crook	DATE		TITLE	ebsa110 6		
DESIGN		DATE					
TOP DOCUMENT NUMBER		SIZE	B	CODE	NUMBER		REV. B

# DRAM SIMMS & address MUX

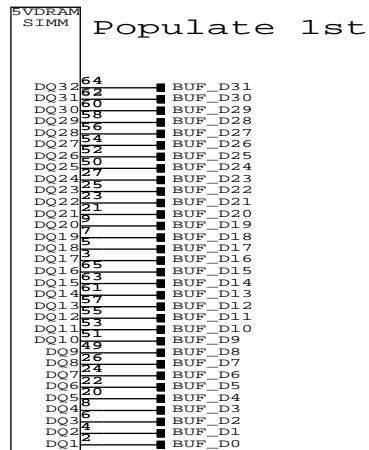
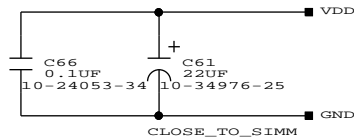
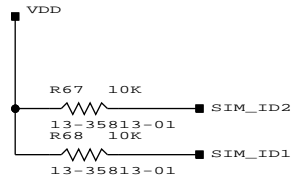
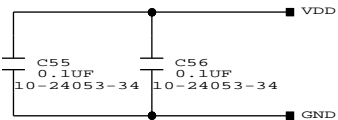
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SIM_ID2	SIM_ID1	Size
0	0	1Mx32
0	1	not supported
1	0	4Mx32
1	1	2Mx32

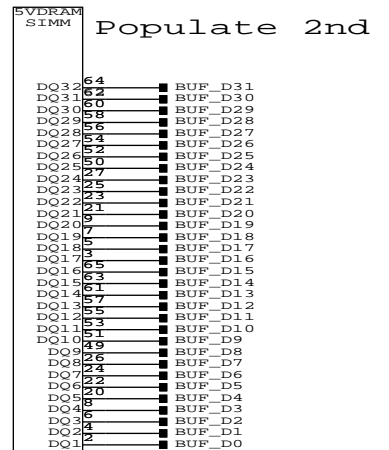
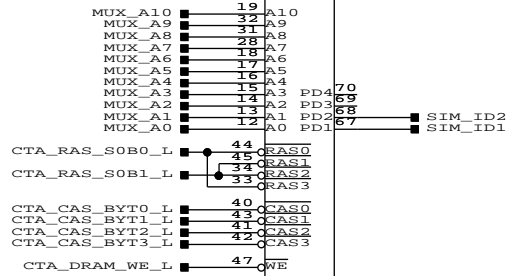
This is the 162260, which has internal 25R resistors on the \*B\* ports. The 1B (COL) path is FASTER (by 0.7ns, around 10%) from SEL transition than 1B.



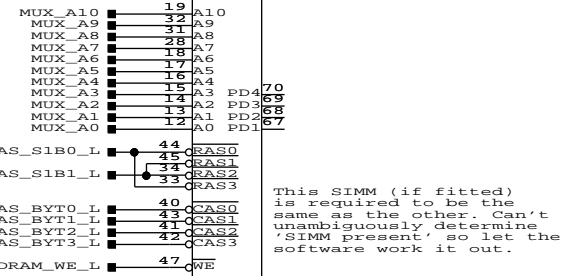
74ABT162260  
21-40545-01  
GND: 4, 11, 18, 25, 32, 39, 46, 53  
VDD: 7, 22, 35, 50



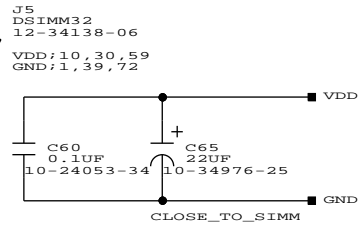
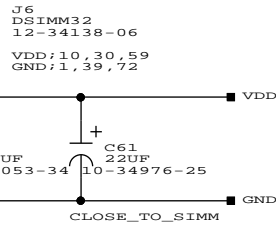
Populate 1st



Populate 2nd



This SIMM (if fitted) is required to be the same as the other. Can't unambiguously determine 'SIMM present', so let the software work it out.



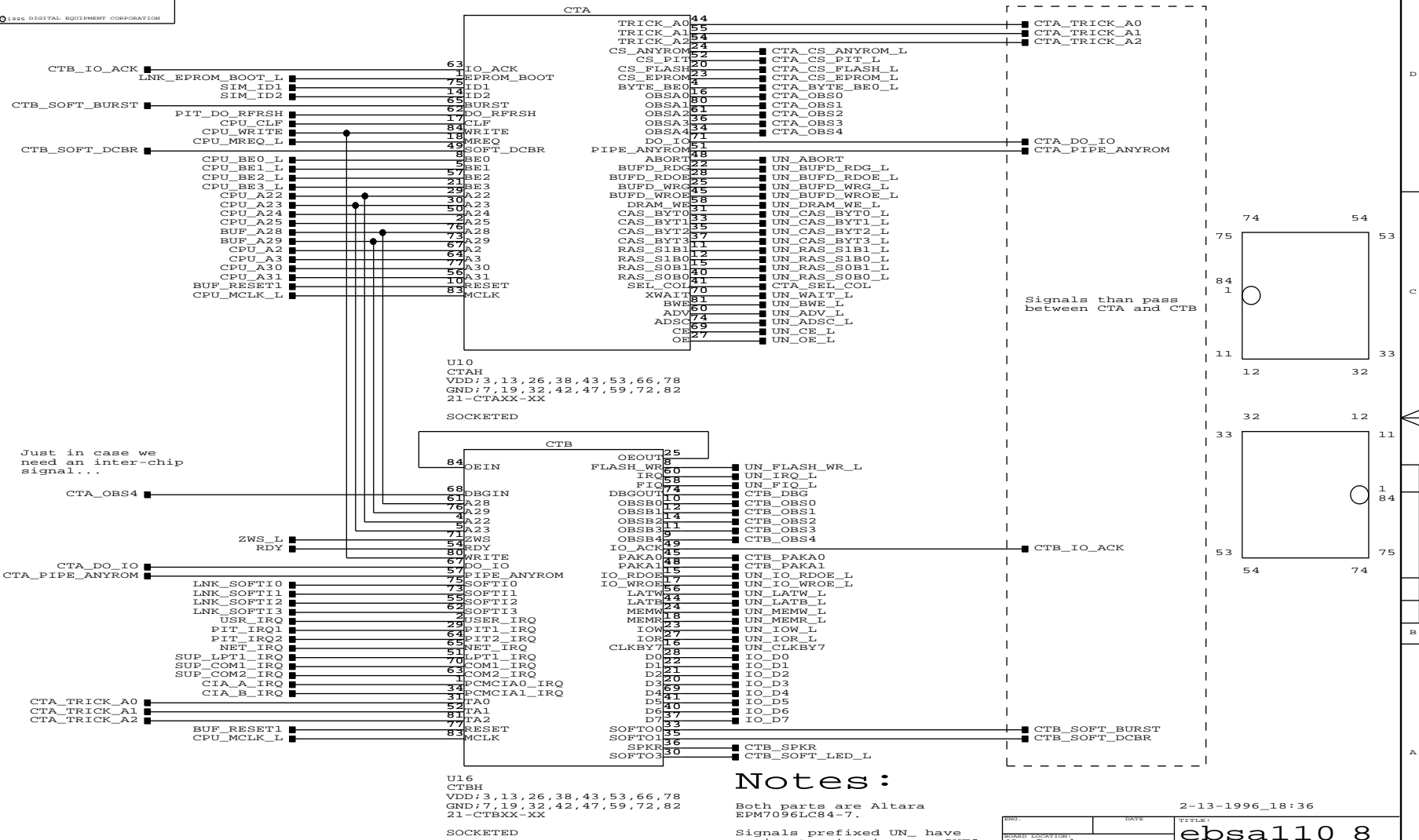
This is the DPN for the 72-pin socket.

2-13-1996\_18:35

DESIGNER: N. Crook	DATE:	TITLE: ebsa110 7
BOARD LOCATION:	OP:	
TOP DOCUMENT NUMBER:	SIZE: B	CODE: NUMBER: REV. B

# Control logic for SSRAM, DRAM, RFRSH, I/O.

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Signals that pass between CTA and CTB

Just in case we need an inter-chip signal...

## Notes:

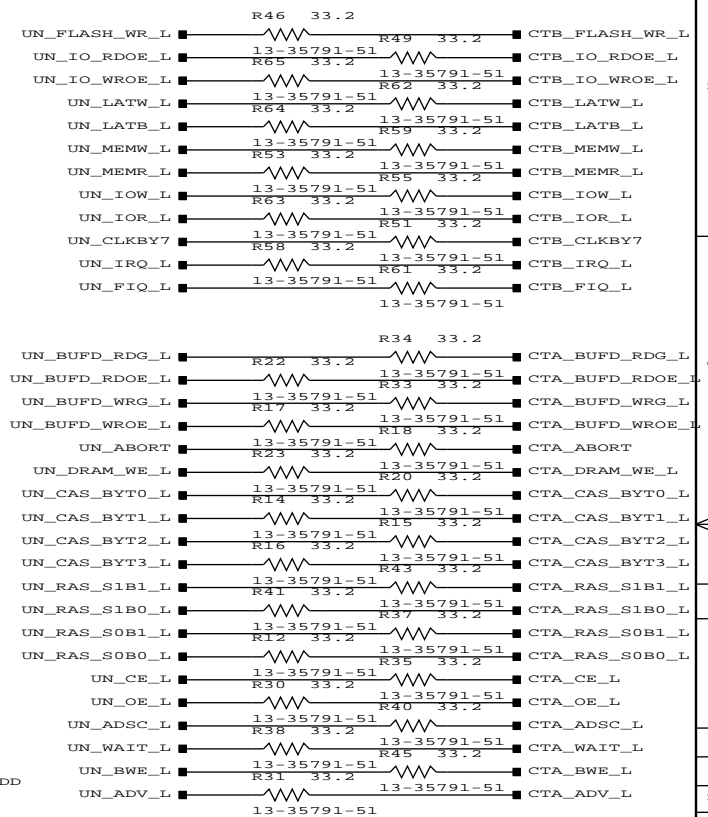
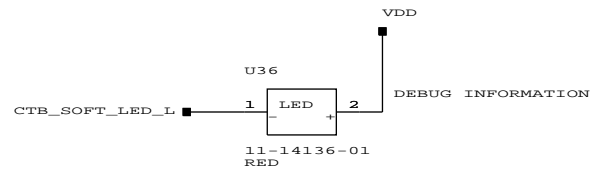
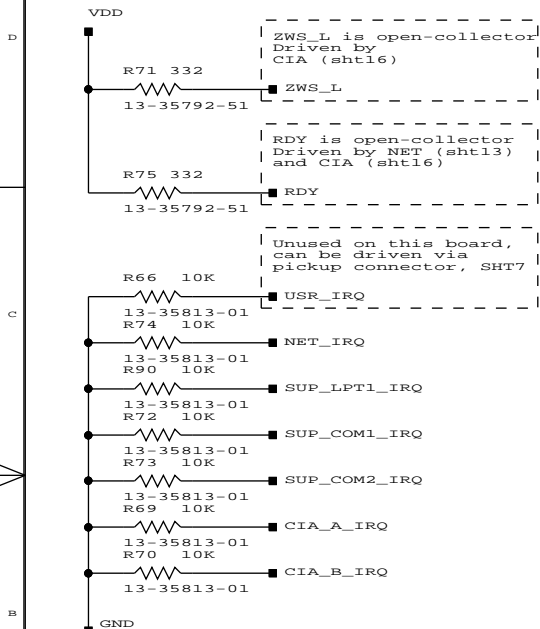
Both parts are Altara EPM7096LC84-7.  
 Signals prefixed UN\_ have series terminations on SHT9.  
 Decoupling is on SHT9.

2-13-1996\_18:36

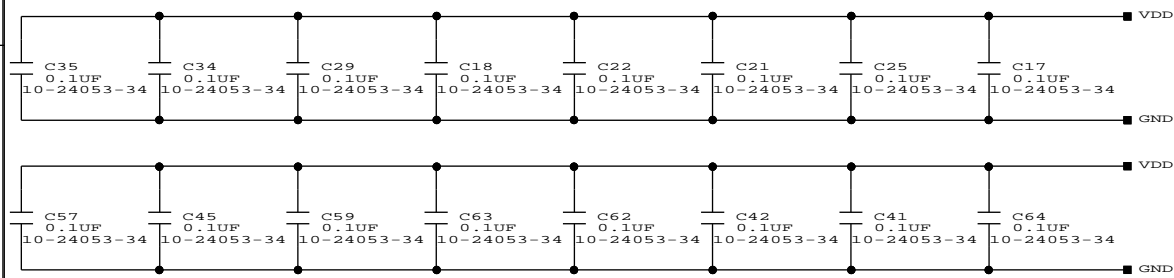
DATE	TITLE		
DESIGNER	ebsa110 8		
REV. C	OP	SIZE	NUMBER
TOP DOCUMENT NUMBER	B	CODE	REV. B

# Control logic: terminations and decoupling

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## Decoupling for CTA, CTB on SHT8



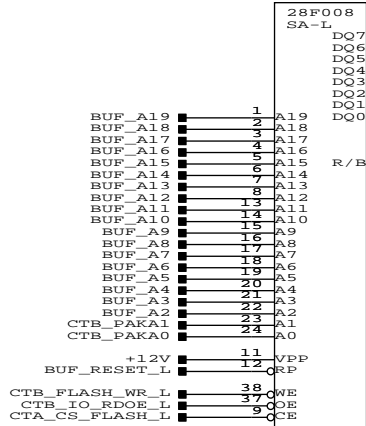
2-23-1996\_11:13

DESIGNER: N. Crook	DATE:	TITLE: <b>esbsa110 9</b>	
DRAWN:	DATE:	SIZE: B	CODE:
TOP DOCUMENT NUMBER:	DATE:	NUMBER:	REV. B

# EPROM packer

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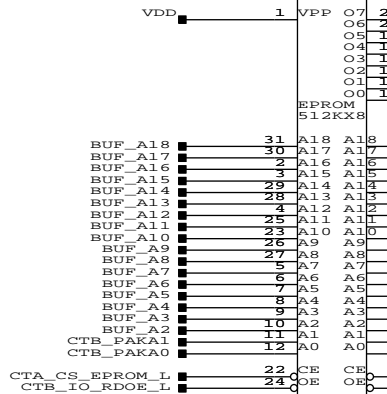
## FLASH



Note: This is NOT pin compatible with the 4Mbit part!  
This IS pin compatible with the 5V-only Am29F080 part. The AMD part has a different programming algorithm and its VPP pin is NC.

U25  
FLASH-8MEG  
VDD;10,31  
GND;29,30  
23-000Z5-03

## EPROM

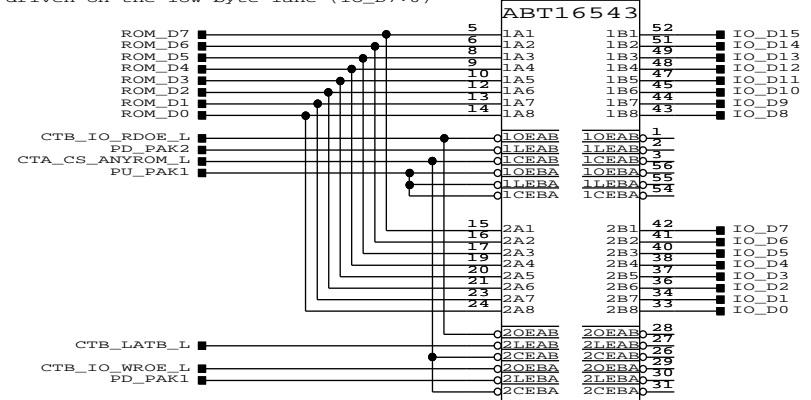


Note: Access time is 150ns or better

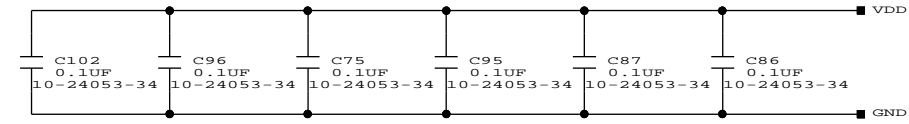
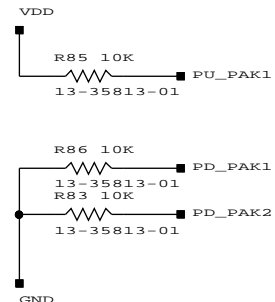
U22  
23-000ED-04  
SOCKETED

For READS, even-address bytes are latched into IO\_D7:0 using LATB. This produces 16-bit values on IO\_D which are packed into 32-bit values by the latches on sht6.

For WRITES (to Flash only), data is always driven on the low byte lane (IO\_D7:0)



U23  
SN74ABT16543  
VDD;7,22,50,35  
GND;4,11,18,25  
21-39191-01



2-13-1996\_18:36

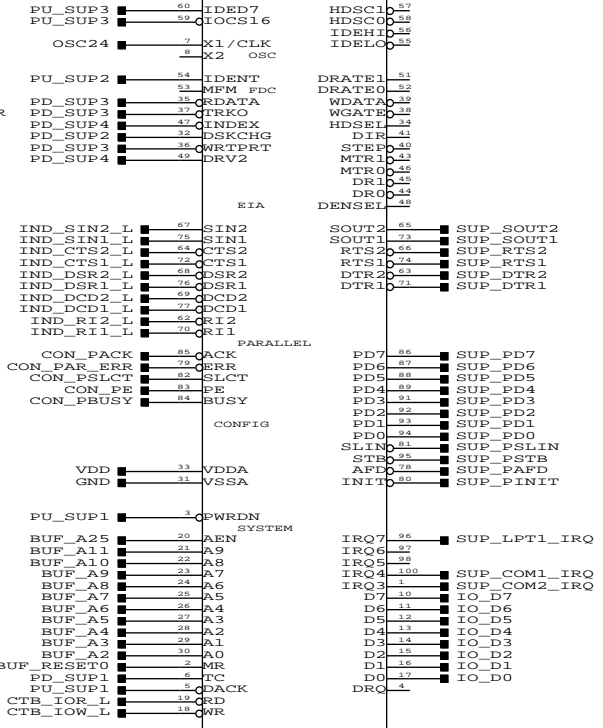
DESIGNER N. Crook	DATE	TITLE ebsa110 10
BOARD LOCATION	OP	NUMBER
TOP DOCUMENT NUMBER	SIZE B	REV. B

# Super I/O

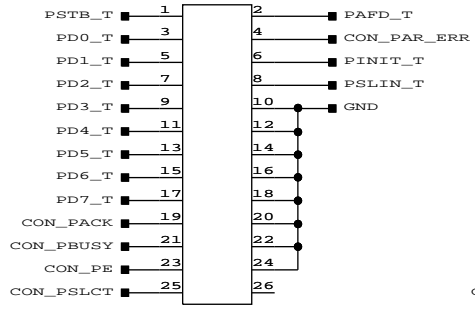
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# National PC87312 Combo chip

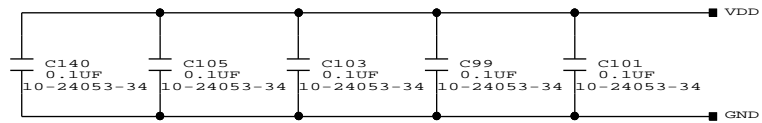
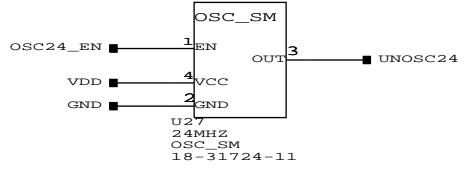
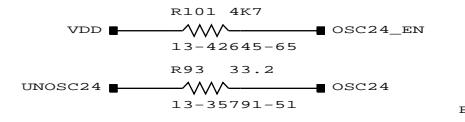
## 87312 HARD DRIVE



## LPT1



J24  
12-23982-10

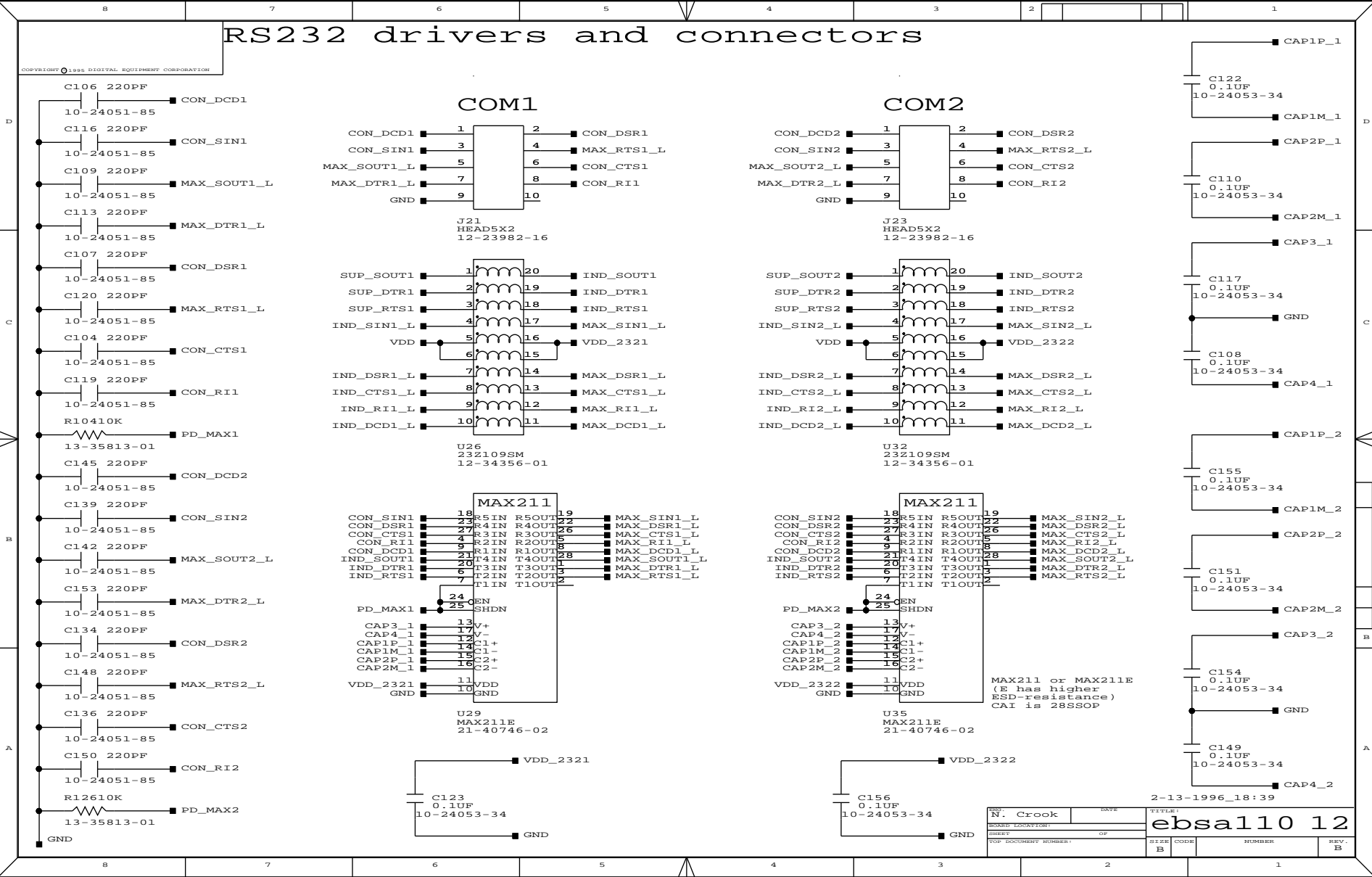


2-13-1996\_18:39

DESIGNER N. Crook	DATE	TITLE ebsa110 11
DESIGN LOCATION	OP	SIZE B
TOP DOCUMENT NUMBER	NUMBER	REV. B

# RS232 drivers and connectors

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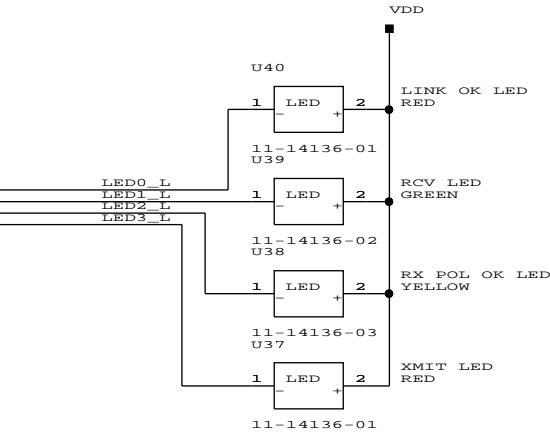
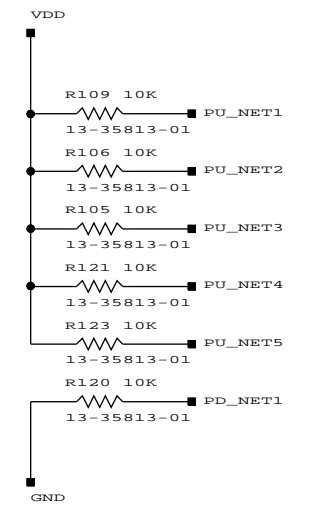
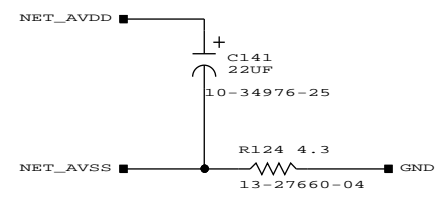
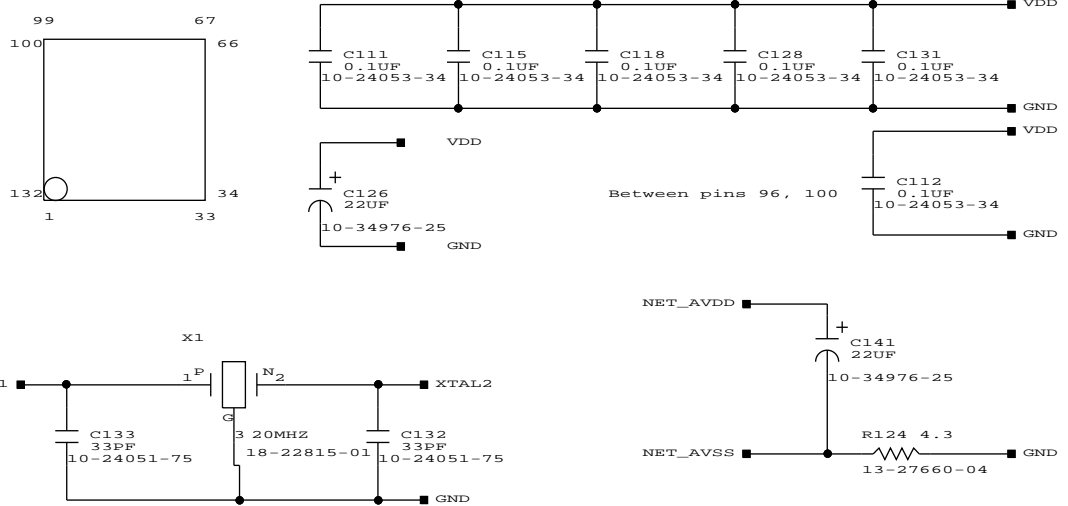
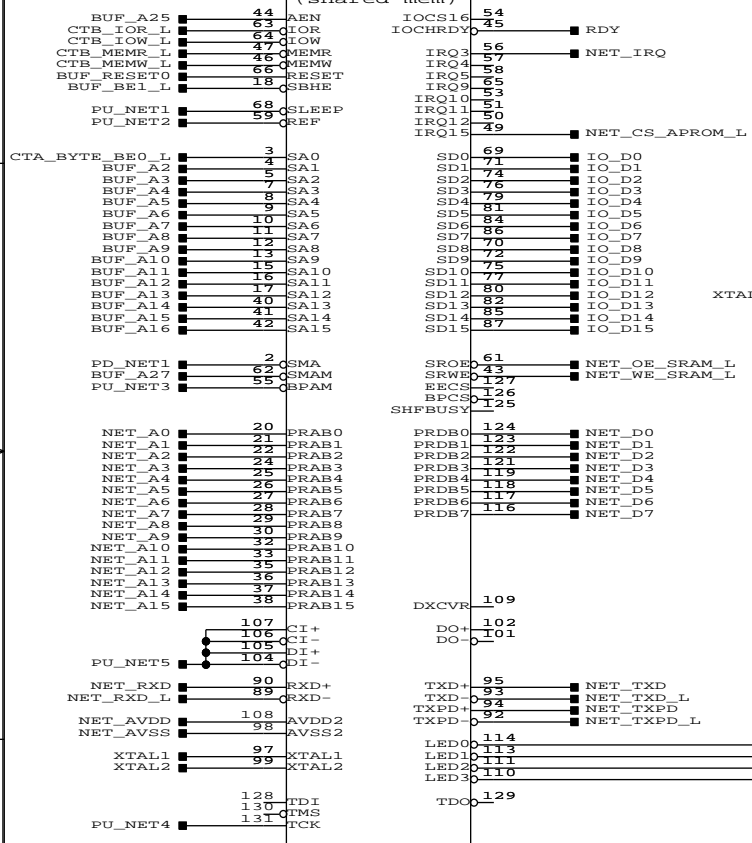
2-13-1996\_18:39

DESIGNER	N. Crook	DATE		TITLE	ebsa110 12		
DESIGN LAYOUT		OP		SIZE	CODE	NUMBER	REV. B
TOP DOCUMENT NUMBER				B			

# Ethernet

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AM79C961A  
(shared mem)



U31  
AM79C961A  
VDD; 19, 34, 52, 67, 78, 115, 132  
GND; 1, 6, 14, 23, 31, 39, 48, 60  
GND; 73, 83, 88, 112, 120  
VDD; 91, 96, 103  
GND; 100  
21-79C96-1A

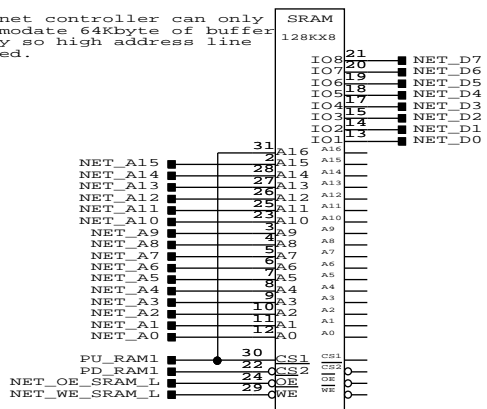
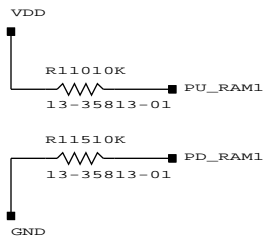
DESIGNER N. Crook	DATE	TITLE ebsa110 13
SHEET LOCATION OP	SIZE B	NUMBER B
TOP DOCUMENT NUMBER	REV. B	

2-23-1996\_11:14

# Ethernet buffer RAM and ID ROM

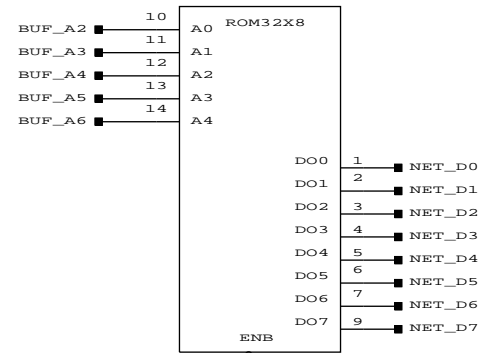
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Ethernet controller can only accommodate 64kbyte of buffer memory so high address line is tied.

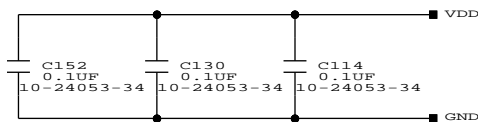


U30  
1 RAM128KX8  
21-31191-04  
STD  
VDD: 32  
GND: 16

23-365A1-00



U33  
NET\_CS\_APROM\_L  
VDD: 16  
GND: 8



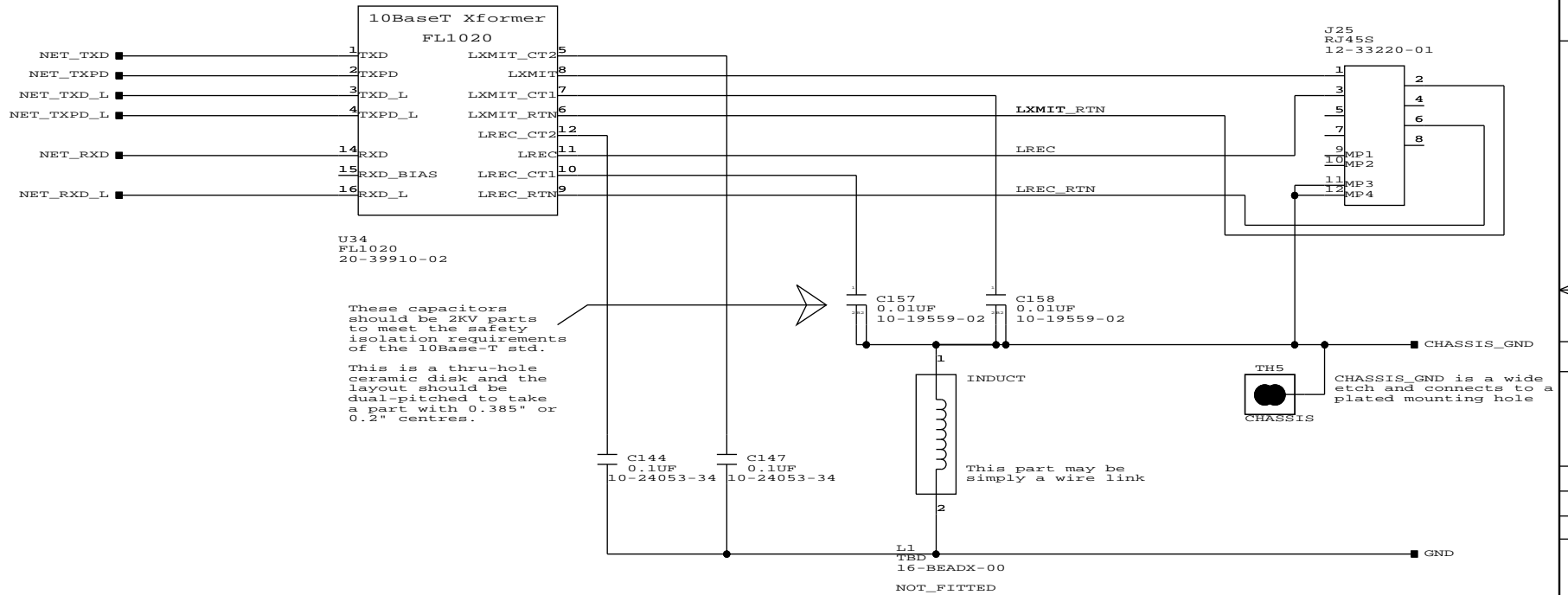
2-23-1996\_11:16

DESIGNER N. Crook		DATE		TITLE 1	
WORK LOCATION		OFF		ebsa110 14	
TOP DOCUMENT NUMBER		SIZE B	CODE	NUMBER	REV. B

# Ethernet - BalUn and media connection

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Wide tracks, no power/ground plane.



2-13-1996\_18:39

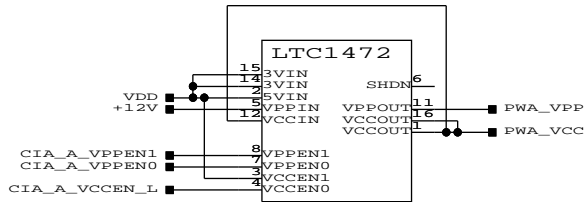
DESIGNER N. Crook	DATE	TITLE etsa110 15
BOARD LOCATION	OP	
SHEET	SIZE B	CODE
TOP DOCUMENT NUMBER	NUMBER	REV. B



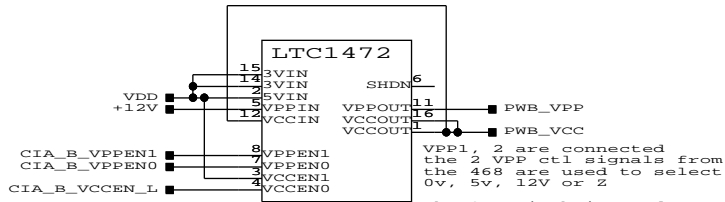
# PCMCIA connectors and power control

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The RFU and RFSH pins are not connected. RFU is reserved and RFSH is named but not defined in spec V2.01



U20  
LTC1472CS  
VDD;9  
GND;10,13  
21-43723-01

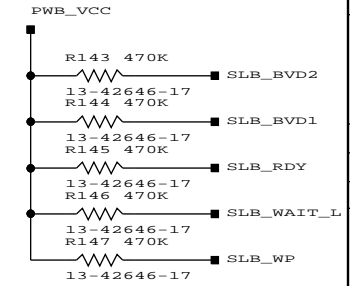
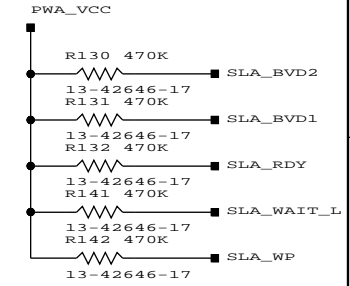
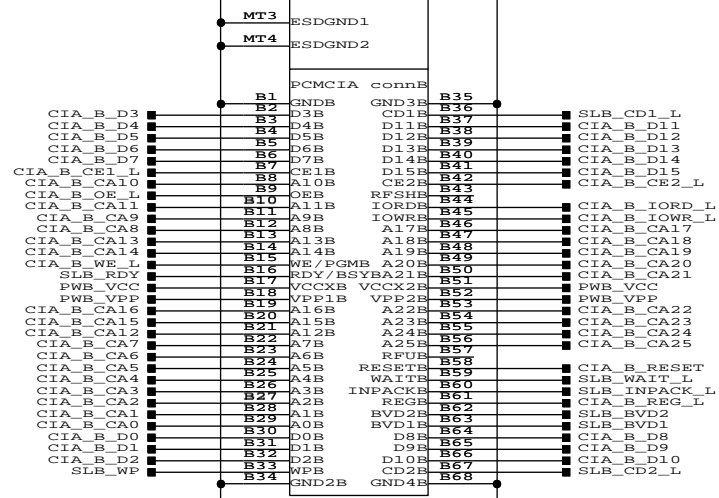
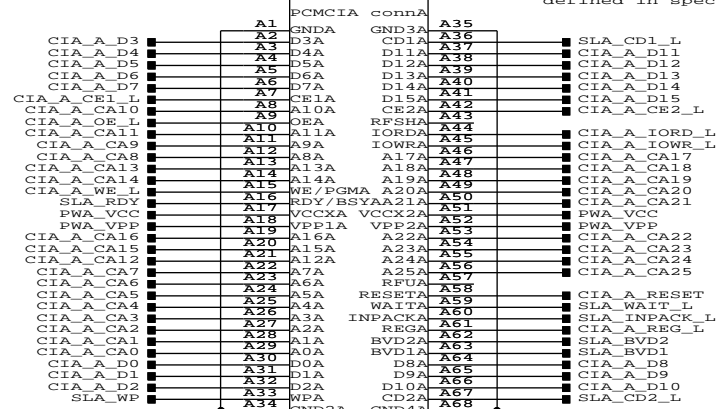
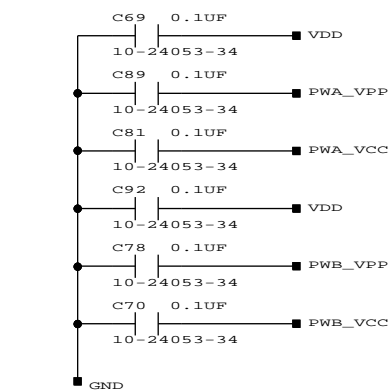


U17  
LTC1472CS  
VDD;9  
GND;10,13  
21-43723-01

VPP1, 2 are connected from the 2 VPP ctl signals from the 468 are used to select 0v, 5v, 12V or Z

The 3V switch is used to route the 5V, because it allows VCCEN\_L to be used (active low)

VCCEN_L	VCC	
0	5V	
1	0V	
VPPEN1	VPPEN0	VPP
0	0	0V
0	1	12V
1	1	5V
		Z



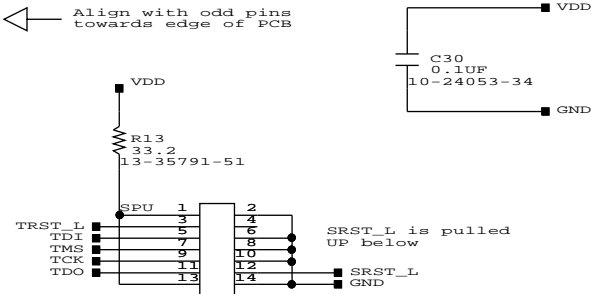
2-13-1996\_18:39

DESIGNER	N. Crook	DATE		TITLE	ebsa110 17		
DESIGNED		DATE					
CHECKED		DATE					
TOP DOCUMENT NUMBER		SIZE	B	CODE	NUMBER		REV. B

TWO\_PARTS

# JTAG port (to CPU only)

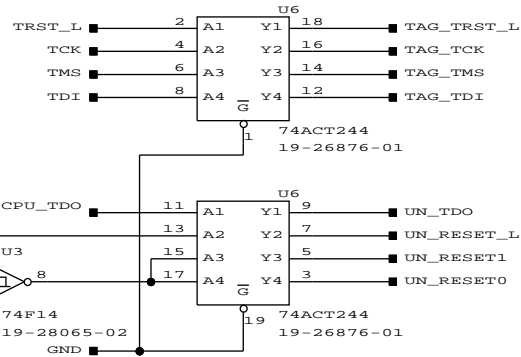
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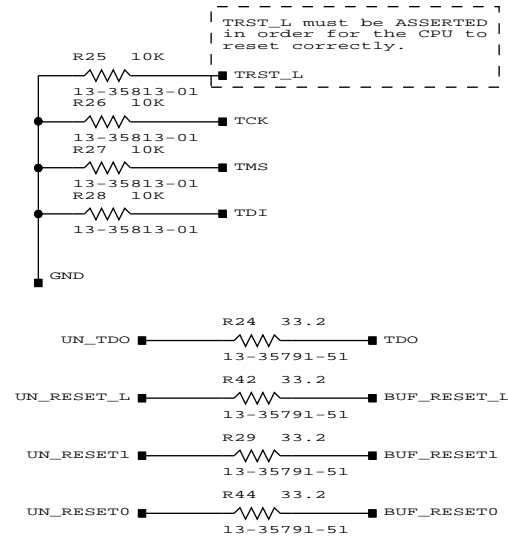
The connected system drives OUT on TDI, and so that signal is routed to TDI on the CPU  
NOT FITTED  
The connected system draws enough power through SPU to power an HC buffer.

SRST\_L is an optional, open-drain signal. The connected system asserts SRST to reset this board. It can be driven and monitored by the connected system.

This connector can run at +5V or +3V. Since it can be live-inserted, it seems safest to have some buffers here, to protect the CPU. It is easiest to power the buffer from +5V and therefore the TAG signals run at 5V and are level-shifted on SHT1



BUF\_RESET\_L used on Flash (SHT10) and debug (SHT4)  
BUF\_RESET1 used on CTA, CTB (SHT8)  
BUF\_RESET0 used on SuperIO (SHT11), Ethernet (SHT13) and PCMCIA (SHT16)

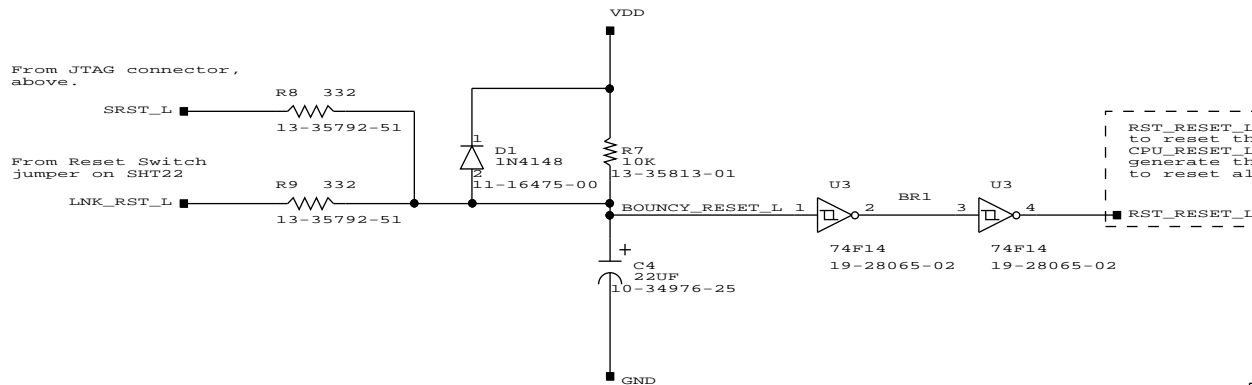


TRST\_L must be ASSERTED in order for the CPU to reset correctly.

# Reset

From JTAG connector, above.

From Reset Switch jumper on SHT22

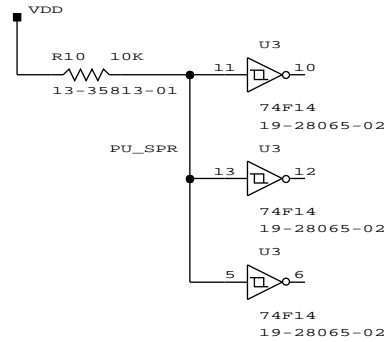


RST\_RESET\_L is level converted (SHT3) and used to reset the CPU (SHT3). The CPU generates CPU\_RESET\_L which is buffered (above) to generate the BUF\_reset signals that are used to reset all the logic on the board.

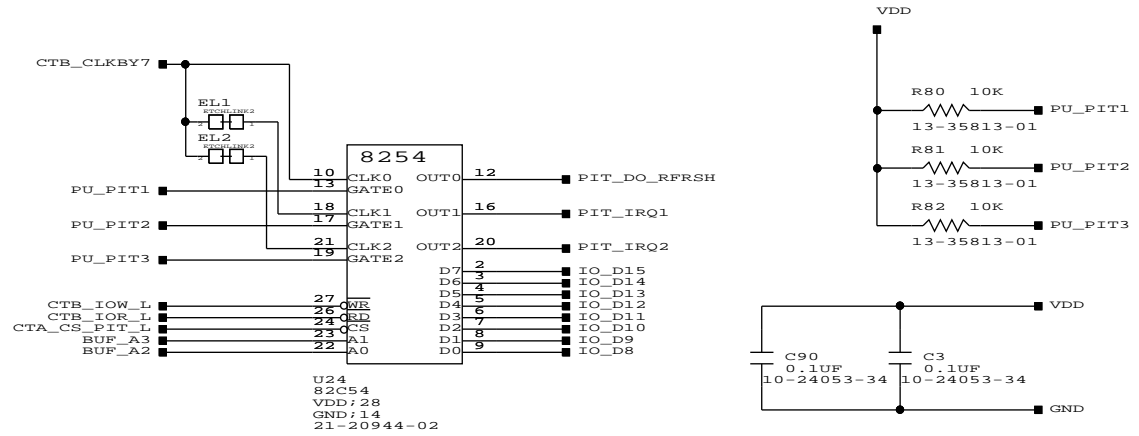
2-15-1996\_17:00

DESIGNER N. Crook	DATE	TITLE ebsa110 18		
DESIGNED BY	DATE	SIZE B	CODE B	NUMBER
TOP DOCUMENT NUMBER				REV. B

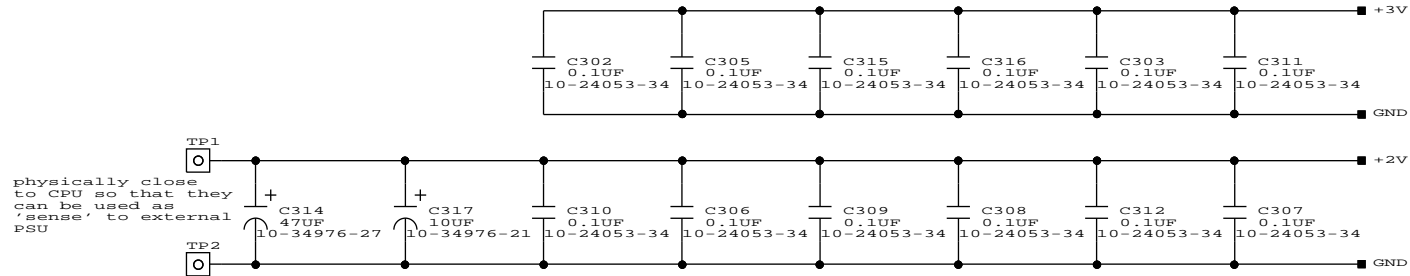
## Spares



## Counter/timer



## Decoupling for CPU (sht 3)

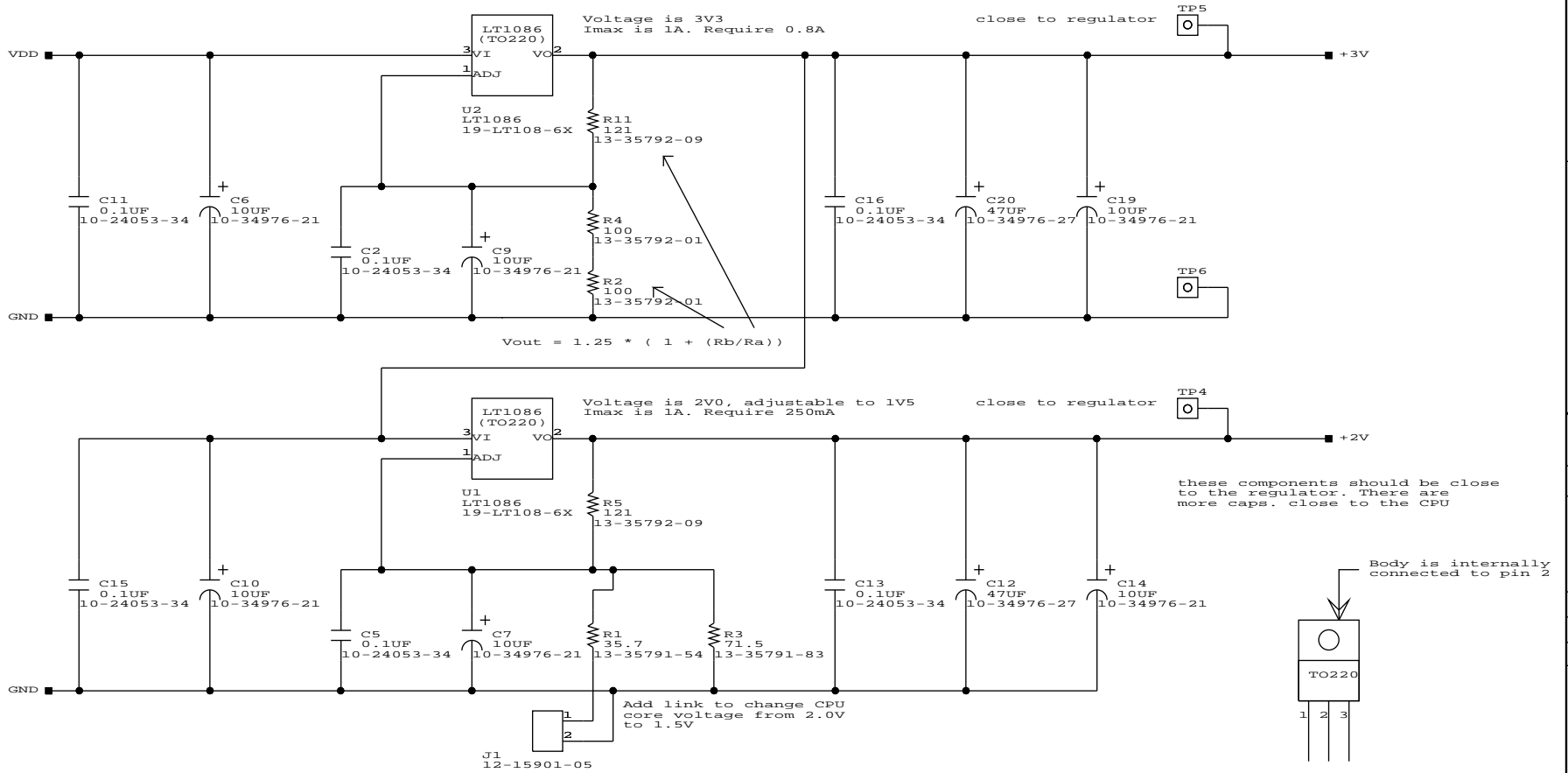


2-13-1996\_18:38

N. Crook		DATE	TITLE	
BOARD LOCATION		ebsa110 19		
DESIGN		OP	SIZE	CODE
TOP DOCUMENT NUMBER		B	NUMBER	REV. B

# Power regulation (3V3, 1.5V/2V)

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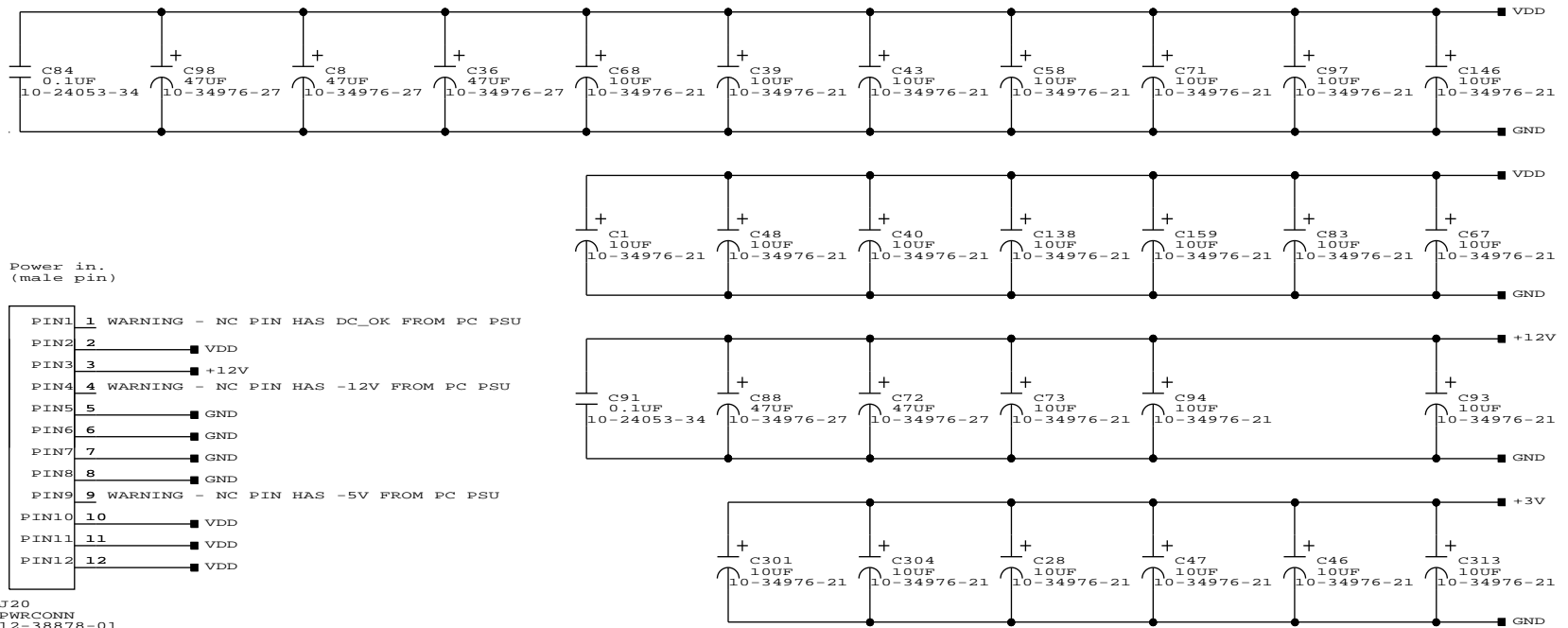
heatsinks \*\*

2-13-1996\_18:39

DESIGNER: N. Crook	DATE:	TITLE: ebsa110 20
WORK LOCATION:	OFF:	
TOP DOCUMENT NUMBER:	SIZE: B	CODE: NUMBER: REV.: B

# Decoupling; bulk, for all power planes

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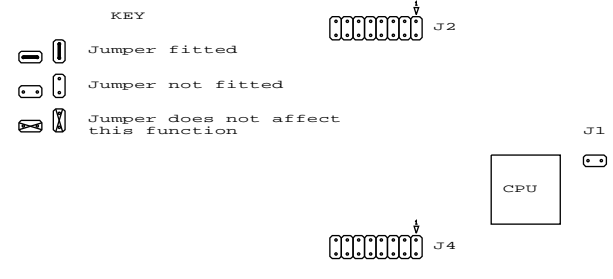
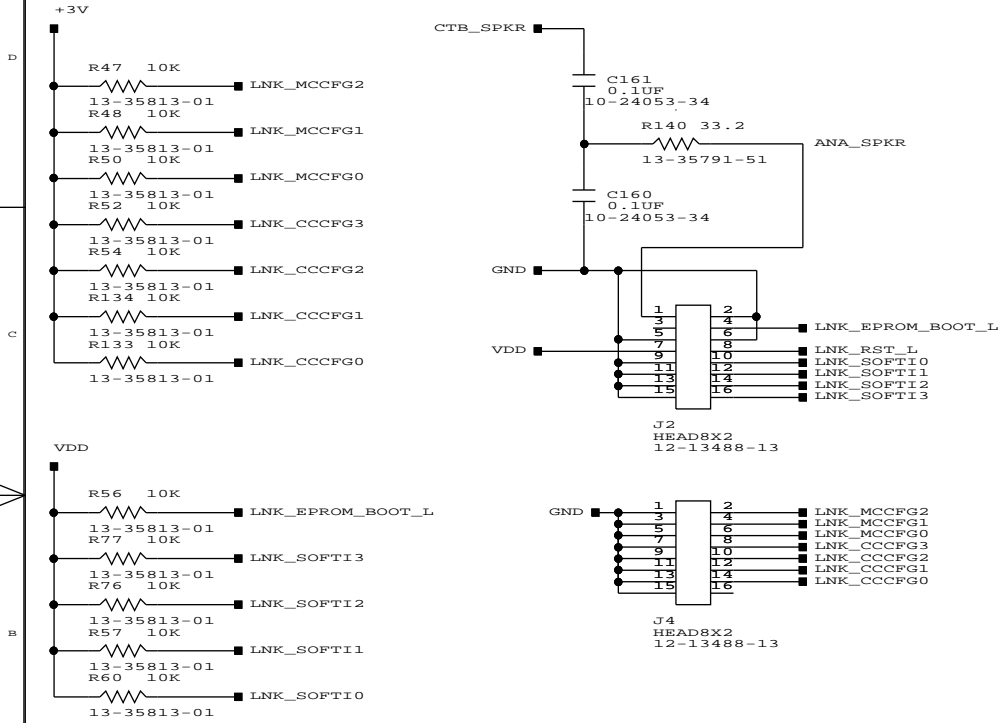
Note: +12V is 'optional'. The board will function with +5V only. +12V is required for programming the FLASH and may be required by a plug-in PCMCIA card.

2-13-1996\_18:39

DESIGNER: N. Crook	DATE:	TITLE: ebsa110 21
BOARD LOCATION:	OP:	
TOP DOCUMENT NUMBER:	SIZE: B	CODE: NUMBER: REV.: B

# Configuration Jumpers (See also SHT20)

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J1	J4	Vcore	Fcore	Fbus	J2	Speaker
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	88.3MHz	44.1MHz	<input checked="" type="checkbox"/>	Speaker TURBO Switch RESET switch
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	95.6MHz	47.8MHz	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	99.4MHz	49.7MHz	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	106.7MHz	53.3MHz	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	143.5MHz	47.8MHz	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	150.9MHz	50.3MHz	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	161.9MHz	53.9MHz	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	+1.5V	169.3MHz	42.3MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	191.3MHz	47.8MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	202.4MHz	50.6MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	213.4MHz	53.3MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	228.1MHz	45.6MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	242.8MHz	48.5MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	257.6MHz	51.5MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	276.0MHz	46.0MHz	<input checked="" type="checkbox"/>	
<input type="checkbox"/>	<input checked="" type="checkbox"/>	+2.0V	287.0MHz	47.8MHz	<input checked="" type="checkbox"/>	

3-1-1996\_10:38

DESIGNER N. Crook	DATE	TITLE ebsa110 22
DESIGN LOCATION	OP	
TOP DOCUMENT NUMBER	SIZE B	CODE
	NUMBER	REV. B