digital

SA-1100
StrongARM
160, 220 MHz

DIGITAL Semiconductor SA-1100 Microprocessor for Embedded Applications Product Brief

The DIGITAL Semiconductor SA-1100 Microprocessor (SA-1100) is a device targeted to provide high performance computing to embedded applications but at consumer electronics pricing with significant MIPS-per-dollar and MIPS-per-watt advantages. The SA-1100 for embedded applications incorporates a 32-bit StrongARM RISC processor running at 160/220 MHz with a large instruction and data cache, memory-management unit (MMU), and read/write buffers running at 160/220 MHz. In addition, the SA-1100 provides system support logic, multiple serial communication channels, a color/gray scale LCD controller, PCMCIA support for up to two sockets, and general-purpose I/O ports.

Applications

- Screen/web phones
- Point-of-sale terminals
- POTS video phones
- Video kiosks
- Intelligent vending machines
- LCD-based network computers
- Modem controllers in modem banks
- Automobile navigation

Operating Systems

• Microsoft	– Windows CE
• Wind River	– VxWorks
• Lucent	– Inferno
• Sun Microsystems	– JavaOS
• Microware	– OS-9
• Chorus	– Jazz
• Psion	– EPOC32
• Apple	– Newton OS
• JMI	– C EXECUTIVE

Benefits

- Record-breaking high performance with significant MIPS-per-dollar and MIPS-per-watt advantages.
- Maintains power/performance by using independent conditional clocking trees to ensure that only currently required units are clocked and other units remain static.
- Industry-leading price/performance delivers the multimedia and graphics capabilities demanded by digital/analog I/O devices.
- High performance for full host-based web phone (implementing all telephone functions including caller ID, call waiting, digital answering machine, and speaker phone).
- Record-breaking performance with the adoption of interpreted languages.
- Complete suite of software and hardware tools speeds time to market.
- Compatibility with ARM and the availability of key third-party development tools (RTOS) reduces design efforts and cost.

Description

The SA-1100 is a general-purpose, 32-bit RISC microprocessor with a 16KB instruction cache (Icache), an 8KB write-back data cache (Dcache), a minicache, a write buffer, a read buffer, an MMU, an LCD controller, and serial I/O combined in a single chip. The SA-1100 maintains leadership in price/performance and power/performance while supporting a full range of operating systems. The SA-1100 provides high performance computing at reduced system cost, making the SA-1100 ideal for meeting embedded application requirements.

Features

- High performance
  → 180 Dhrystone 2.1 MIPS @ 160 MHz
  → 250 Dhrystone 2.1 MIPS @ 220 MHz
- Low power (normal mode) *
  → <320 mW @2.0 V/160 MHz
  → <450 mW @2.0 V/220 MHz
- Integrated clock generation
  → Internal phase-locked loop (PLL)
  → 3.686-MHz oscillator
  → 32.768-kHz oscillator
- Big and little endian operating modes
- 3.3-V I/O interface
- 208-pin thin quad flat pack (LQFP)
- 32-way set-associative caches
  → 16KB instruction cache
  → 8KB write-back data cache
- 32-entry MMUs
  → Maps 4KB, 8KB, or 1MB
- Write buffer
  → 8-entry, between 1 and 16 bytes each
- Read buffer
  → 4-entry, 1, 4, or 8 words
- Memory bus
  → Interfaces to ROM, Flash, SRAM, and DRAM
  → Supports two PCMCIA sockets

* Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design.

SA-1100 CPU

The SA-1100 CPU implements the ARM V4 architecture as defined in the *ARM Architecture Reference Manual*. Architectural enhancements beyond the ARM V4 are implemented through use of coprocessor 15. Control register reads and writes to coprocessor 15 provide access to MMU, cache, and write and read buffer control registers.

The SA-1100 MMUs provide separate 32-entry translation lookaside buffers (TLBs) for the instruction and data streams. Each of the 32 entries may map segments, large pages, or small pages in memory. The SA-1100 contains 16KB of instruction cache and 8KB of data cache. In addition to this, a minicache is provided to prevent periodic large data transfers from thrashing the main data cache. The data and instruction caches are implemented as 32-byte blocks, and provide 32-way associativity, with victim replacement performed in a round-robin fashion. The minicache is 16 entries and is 2-way set associative, implementing the least-recently-used (LRU) algorithm for victim replacement.

The SA-1100 also provides a write buffer and a read buffer. The read buffer allows critical data to be prefetched under software control, preventing pipeline stalls from occurring during external memory reads. The write buffer provides additional system efficiency by buffering between the CPU clock frequency and the actual bus speed when data is being written by the CPU to external memory. The write buffer is eight entries, and allows each entry to contain between 1 and 16 bytes. The read buffer is four entries, and allows each entry to contain 1, 4, or 8 words.

SA-1100 System Control Functions

The SA-1100 provides timers, power-management functions, interrupt control, reset control, and onchip oscillators and PLLs for clock generation. There are 28 general-purpose I/Os, which can, in addition to being directly read or written by the CPU, be programmed to generate an interrupt.

The real-time clock and trim logic run off the 32.768-kHz crystal and provide accuracy of ±5 seconds/month.

The 32-bit OS timer runs off the 3.686-MHz oscillator and is used in companion with the four 32-bit timer match registers. One of the four match registers is used specifically as a watchdog timer interrupt, preventing system lockout from occurring when software or hardware is trapped in a loop state with no controlled exit. The remaining three registers are available for use as interval timers or other user-defined purposes.

The interrupt controller routes all interrupt sources to either an FIQ or IRQ request to the CPU. IRQ is a lower priority interrupt and may be interrupted by FIQ. FIQ is unique to the ARM architecture and allows fast servicing to occur on specific interrupt sources, as determined by the user. There are two levels in servicing interrupts. The first level alerts the user or operating system to what specific module on the SA-1100 experienced an interrupt condition. The second level provides information on what event within the specific module caused an interrupt to be flagged.

The reset controller manages the various reset sources within the SA-1100 and provides the ability to invoke a software reset. In addition, the reset controller tracks the cause of the last known reset, whether a hard reset, soft reset, watchdog timer expiration, or sleep mode reset.

The SA-1100 provides 28 general-purpose I/O pins, which may be programmed to generate interrupts on rising, falling, or both edges. The GPIO pins may be toggled under CPU control at 50 MHz for a 220-MHz processor. The user is given the option of utilizing a subset of the GPIO pins to support extra functionality in either the serial channels or the LCD controller but may choose to use some, all, or none of the added functionality.

SA-1100 Memory Control Module

The SA-1100 contains a flexible memory controller that can access DRAM, EDO DRAM, SRAM, Flash, and ROM. The SA-1100 memory map supports up to four banks of DRAM; each bank provides 128MB of addressable space allowing both currently available and future memory densities to be supported. The DRAM controller supports CBR as well as self-refresh DRAM. Burst reads occur in 1, 2, 3, 4, or 8 words (beats) as determined by the data destination within the SA-1100 (cache line fill, read buffer, or DMA). Burst writes occur in 1, 2, 3, 4, or 8 words, depending on the final destination of the data outside the SA-1100 (write buffer, DMA). When a castout is occurring from cache, the

Block Diagram of the SA-1100

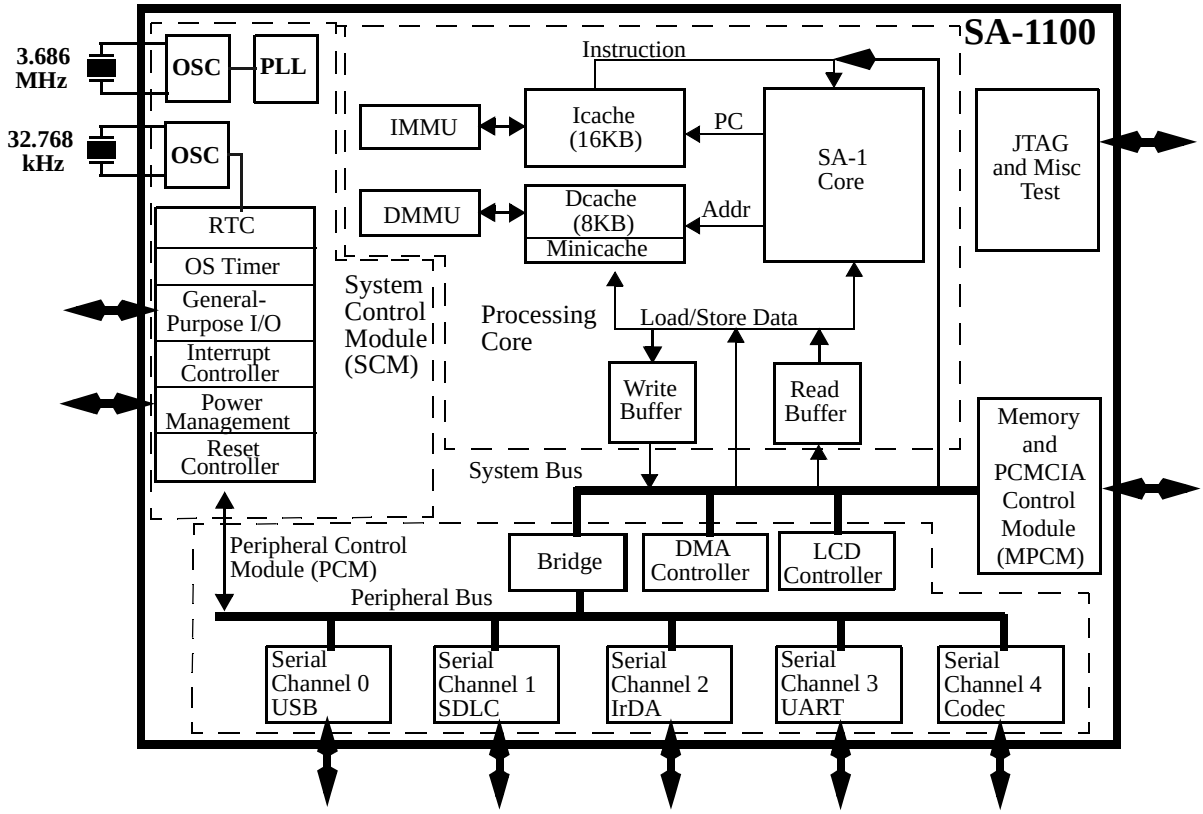

Table 1 Additional Features Built into SA-1100

	160 MHz	220 MHz
Performance	180 MIPS	250 MIPS
Supply	2.0 V	2.0 V
USB	12 Mb/s	12 Mb/s
IrDA	115 Kb/s, 4 Mb/s	115 Kb/s, 4 Mb/s
SDLC	230 Kb/s	230 Kb/s
UART	230 Kb/s	230 Kb/s
Codec	UCB1100, UCB1200, SPI, TI, µWire	UCB1100, UCB1200, SPI, TI, µWire
LCD	1-, 2-, 4-, 8-, 12-, 16-bits/pixel	1-, 2-, 4-, 8-, 12-, 16-bits/pixel
Memory	EDO, DRAM, ROM, Flash, SRAM	EDO, DRAM, ROM, Flash, SRAM
Interrupt	FIQ, IRQ, Wake-up	FIQ, IRQ, Wake-up

SA-1100 will perform an 8-word write for a full 32 bytes.

Included in the SA-1100 memory controller is support for up to two slots of PCMCIA. The implementation shares address and data pins with the memory controller. Access speeds to PCMCIA memory and I/O are user-programmable. Some external buffering is required for this interface.

SA-1100 Peripheral Control Module

The SA-1100 contains a six-channel DMA controller to support the high-speed data movement inherent in serial communications. Note that the LCD controller contains its own independent DMA channels, and that the six DMA channels are available for use by the other peripheral I/O functions. The DMA controller is dedicated to data movement between the serial channels and external memory, whether DRAM, SRAM, Flash, or ROM.

The LCD controller on the SA-1100 supports up to 256 colors and 16 gray-scale levels, on a single or split-screen display with resolution up to 1024 X 1024. The LCD controller is implemented using a patented dithering algorithm controlling the intensity of the information displayed. In the case of color, the dithering algorithm controls which 256 of the 4096 available colors are displayed during any given frame. Frame buffer data is used by the LCD controller as an address value, which is then decoded as an index into a 256-entry by 12-bit wide

palette RAM. If 12-bit data is required, the palette RAM may be bypassed and frame buffer data passes directly to the dither logic. If 16-bit data is required, both the palette RAM and the dither logic are bypassed, and data is sent directly to the LCD controller pins. The LCD controller supports both TFT and STN panels.

Serial port 0 on the SA-1100 implements the universal serial bus (USB) slave protocol, supporting three endpoints operating at 12 Mb/s, half duplex.

Serial port 1 on the SA-1100 implements either the synchronous data link controller (SDLC) or universal asynchronous receiver-transmitter (UART), both at baud rates up to 230 Kb/s. If both SDLC and UART are required in a given system, two GPIO pins can be configured to perform the UART RX/TX functionality, leaving the TX_2/RX_2 pins free for SDLC.

Serial port 2 on the SA-1100 provides logic to support IrDA at either 115 Kb/s or 4 Mb/s. The low-speed IrDA utilizes the HP-SIR standard, and the high-speed IrDA implements the 4 PPM standard.

Serial port 3 on the SA-1100 is a UART channel operating from 56.24 b/s to 230 Kb/s. Modem control signals may be implemented via the GPIO pins if required, but for maximum flexibility these signals are not predefined.

Serial port 4 on the SA-1100 also implements a multimedia communications port or synchronous serial port (MCP/SSP). These ports are traditionally used for interfacing to specific digital/analog I/O devices such as codecs, keyboards, touchpads, audio and record/playback. If required, the SA-1100 provides the user with an option to support both the MCP as well as SSP by dedicating two GPIO pins to the SSP.

The MCP gluelessly interfaces to the Philips UCB1200, which provides support for both audio and telecom codecs as well as a touchpad interface and 10 general-purpose I/O pins. The SA-1100 contains two pairs of transmit and receive FIFOs to support the telecom and audio data. The SA-1100 also provides two 21-bit data registers, one each for receive and transmit codec data. The SSP logic interfaces to devices that support the National MicroWire protocol, the Texas Instruments synchronous serial protocols, as well as a subset of the Motorola SPI protocol. All of these protocols provide methods to interface to keyboard drivers, serial EPROMs, ADC/DAC, as well as special-purpose devices such as voice record/playback. The SSP functions as a master only, communicating to offchip devices by driving a serial bit-rate clock ranging from 7.2 kHz to 1.8432 MHz, and supports data formats from 4 to 16 bits in length.

Table 2 SA-1100 Tool Chains and Operating Systems

Manufacturer	Operating System	Tool Chain
Microsoft	Windows CE	Visual C/C++
Wind River	VxWorks	Tornado
Lucent	Inferno	Inferno Toolkit
Sun Microsystems	JavaOS	JDK, JavaWorks
Microware	OS-9	FasTrac
Chorus	Jazz	C++ compilers
Psion	EPOC32	GNU
Apple	Newton OS	Newton Developer Tools
JMI	C EXECUTIVE	Multiple sources
Integrated Systems	pSOS	pRISM+

SA-1100 Test and Debug Support

The SA-1100 provides debug support via instruction and data breakpoints. These are user-programmable and are implemented through the coprocessor instructions. In the case of an instruction breakpoint, the user may halt the processor after execution of an instruction at a specific address. The data breakpoint allows a user to halt on a specific data pattern as well as on the reference address to that data pattern. There is a data breakpoint mask register that provides further qualification on specific data.

The SA-1100 also provides a JTAG interface, which has been specifically targeted to provide continuity checking for system designs. Supported instructions include EXTEST, SAMPLE/PRELOAD, CLAMP, BYPASS, HIGH-Z, and IDCODE.

SA-1100 Tool Chains and Operating Systems

The SA-1100 has an extensive list of supporting operating systems and tool chains. See Table 2 for a subset of the available operating systems.

SA-1100 Power Benefits

The SA-1100 continues the StrongARM family legacy of record-breaking low-power performance by consuming 320 mW @ 160 MHz and 450 mW @ 220 MHz. The SA-1100 takes advantage of a 2.0-V nominal process technology and provides the industry's leading technology solution for tethered products. The I/O ring runs at 3.3 V to allow simple system interconnections. Another key element in the SA-1100 power strategy is the use of independent conditional clocking trees, which ensure that only currently required units are

clocked and other units remain static. The SA-1100 may be run at a variety of frequencies, ranging from 39 MHz up to 220 MHz.

SA-1100 Performance Benefits

The SA-1100 provides high-end desktop performance to the embedded application market without sacrificing power or price. Applications utilizing the SA-1100 are able to take advantage of technology such as Softmodem, speech recognition, and text-to-speech without a reduction in user-interface performance. Use of the performance-intensive Softmodem algorithm can provide up to $20 savings in overall system cost. When running on the SA-1100, a Softmodem requires less than 30% of the processor bandwidth, ensuring that none of the other SA-1100 functions, including LCD display and serial channel operation, experience a degradation in performance.

Another advantage to the performance provided by the SA-1100 becomes apparent with the adoption of interpreted languages. An example of this is demonstrated by comparing the CaffeineMark performance of the SA-1 core on the SA-1100 to other competing parts in the market. The SA-1 core outperformed processors more than 10 times the price of the SA-1100 when running Java.

SA-1100 Characteristics

	SA-1100 160 MHz	SA-1100 220 MHz
Clock	160 MHz	220 MHz
V2.1 Dhrystone MIPS	180	250
Core power supply	**Vss** = 0.0 V dc **Vdd** = 2.0 V dc ± 10%	**Vss** = 0.0 V dc **Vdd** = 2.0 V dc ± 5%
I/O power supply	**Vssx** = 0.0 V dc **Vddx** = 3.3 V dc ± 10%	**Vssx** = 0.0 V dc **Vddx** = 3.3 V dc ± 10%
Power dissipation *	<320 mW	<450 mW
Ambient operating temperature	Standard = 0°C (32°F) min. 70°C (158°F) max. Extended = –20°C (–4°F) min. 70°C (158°F) max.	Standard = 0°C (32°F) min. 70°C (158°F) max. Extended = –20°C (–4°F) min. 70°C (158°F) max.
Storage temperature	–40°C to +125°C (–40°F to +257°F)	–40°C to +125°C (–40°F to +257°F)
Packaging Process technology Transistor count	208-pin LQFP ** .35 µm, 3-layer metal 2.5 million	208-pin LQFP ** .35 µm, 3-layer metal 2.5 million
Order number	DE–S1100–CA	DE–S1100–DA

* Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design.

** DIGITAL Semiconductor has modified its package nomenclature due to industry standardization of packages. LQFP is 1.4 mm thick, thin quad flat pack. Please note that no modification has been made to the package itself.

For More Information

To learn more about the availability of the StrongARM SA-1100 Microprocessor, contact your local semiconductor distributor. To learn more about DIGITAL Semiconductor's product portfolio, visit the DIGITAL Semiconductor World Wide Web Internet site:

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