



SA-1100 Evaluation Platform Schematics Description

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None Used.

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None Used.

1.0 Introduction

This document describes the SA-1100 microprocessor evaluation platform schematics as the project was sent to the PCB board fabricator. These are **not** the final SA-1100 microprocessor evaluation platform schematics. Some minor tweaks will certainly occur at that time.

The SA-1100 microprocessor evaluation platform is neither a "typical" system nor is it a "reference design." This evaluation platform is a Design Verification Platform for the SA-1100 microprocessor. Designers of SA-1100-based systems should be able to extract the portions of the SA-1100 microprocessor evaluation platform schematics that are relevant to their particular set of design goals.

The SA-1100 microprocessor evaluation platform was designed to allow the SA-1100 to operate in as many modes as possible, and to provide hardware for "lab debug" assist. This evaluation platform assumes that the first SA-1100 being inserted into it is nonfunctional, and could possibly be damaging to other hardware in the system.

1.1 Notes About the SA-1100 Evaluation Platform Schematics

The schematics for the SA-1100 microprocessor evaluation platform were created using the VeriBest Design Capture software running under Windows NT* 4.0.

The date shown in the lower right corner is the date that the files were sent to the board fabricators. Any schematic dated prior to 6/21/97 is considered "preliminary" and is superseded by this set of schematics.

These schematics were drawn hierarchically. Some sheets have no electrical components at all. These sheets are present only to show the interconnect between the blocks.

The name of each block on a hierarchical block corresponds to a schematic with the same name. The schematic name is shown in the lower right corner of each page. The highest level schematic is named Brutus, and is numbered as Sheet 1.

Buses are drawn with a wide line, and all corners on buses are drawn at 45 degree angles. Individual signals are drawn with narrow lines, and all corners are drawn at 90 degree angles.

These schematics have been subjected to very extensive component, gate, and pin swapping while in the physical design environment (VeriBest PCB). These pin and gate swappings have been automatically backannotated onto the schematics. As a result, the numbering of the pins may indeed appear to be "out of order" from the initial (usual) schematic symbol orientation. They are, however, still functionally correct. This reduces the combined estimated trace lengths to these components by 150 inches.

Note: V_{CC} is the same as +5 V.

The SPDT switches used in numerous locations on the SA-1100 microprocessor evaluation platform are the Secme 1K2 slide switches. With the slide in one position, a dot is visible on the physical switch. With the slide in the other position, no dot is visible. When the dot is visible, the switch is connected as shown on the schematic. Where possible, "one dot" creates a high signal level – a one; and "no dot" creates a low signal level – a zero.

The symbols on the schematics do not show the power and ground connections. They are defined in the VeriBest Parts Database. You may, however, determine which power plane the device is connected to by seeing what voltage the decoupling capacitors (located near the symbol) are connected to. When a device could be connected to more than one voltage plane (not simultaneously), then the power pins are drawn on the schematic symbol to show the actual connection.

The triangular symbols with the TPx reference designators are color-coded test points (TP-105 series by Components Corp.). The SA-1100 microprocessor evaluation platform design always uses a black test point for ground, a red test point for a power source, and a yellow test point for a signal of interest.

2.0 SA-1100 Microprocessor Evaluation Platform Schematics

This section briefly explains the SA-1100 microprocessor evaluation platform schematics on a page-by-page basis.

2.1 Sheet 1 – Brutus

The schematic sheet named Brutus is the highest level sheet in the hierarchy. There are no actual electrical components on this page. It effectively displays the partitioning of the SA-1100 microprocessor evaluation platform major functional blocks: clocks, power, processor, memory, peripherals, and a block named "visibility" that provides a built-in logic analyzer connection arrangement.

2.2 Sheet 2 – StrongARM**

The schematic sheet named StrongARM contains the StrongARM SA-1100 microprocessor and its decoupling capacitors. Note that pins 188 and 193 should each have its own dedicated decoupling capacitor. In addition, five yellow test points have been attached to each of the five JTAG boundary-scan signals on the SA-1100, which are otherwise unused in the SA-1100 microprocessor evaluation platform design.

The naming of the signals on this schematic sheet follow the convention used in the SA-1100 specification, except for the 28 GPIO signals. On the SA-1100 microprocessor evaluation platform schematics, they are named according to which GPIO pins that are on the SA-1100, and followed by a slash, and then the alternate function that signal is used for elsewhere in the SA-1100 microprocessor evaluation platform schematics.

Most SA-1100 microprocessor evaluation platform systems will be populated with a Nepenthe QP1-208050-125 socket that accommodates the SA-1100 in the standard TQFP-208 package. A few SA-1100 microprocessor evaluation platform systems will be built with special sockets to accommodate the engineering samples of the SA-1100 in other package types.

2.3 Sheet 3 – Clocks

The schematic sheet named Clocks is the first sheet that vividly displays the design philosophy behind the SA-1100 microprocessor evaluation platform. (That is, the SA-1100 microprocessor evaluation platform was designed to allow the SA-1100 to operate in as many modes as possible, and to provide hardware for "lab debug" assist.)

In virtually any other SA-1100-based system, the only two components needed from this page are the two crystals labelled X2 and X3. Crystal X2 is a Fox NC38 32.768 KHz tuning fork watch crystal. Crystal X3, which is of the AT-cut variety, is a Fox HC80 3.6864 MHz crystal with the standard 20 pF load capacitance.

The TSTCLK_BYP mode control signal on the SA-1100 is set by switch S3, and the external TESTCLK may be applied through the SMA connector labelled J19. When applying TESTCLK, the signal amplitude must remain between GND and 2.4 V.

The remaining circuitry on this page is present for two reasons:

1. To allow the design verification team to vary the frequency of operation of the SA-1100 in the lab.
2. In case the combined capacitance of the SA-1100 socket with switches S5, S6, S9, and S10 render the crystals nonfunctional.

To vary the frequency into the PXTAL input pin on the SA-1100, switches S9 and S10 must both be thrown so that "no dots" are showing, and S8 must be in its "no dot" position. The PXTAL signal may then be driven directly from an external laboratory pulse generator connected to SMA connector J21. The SA-1100 microprocessor evaluation platform provides the proper impedance-terminating resistor for a pulse generator designed to drive into a 50Ω impedance load.

Note: The voltage applied must remain between 0.0 V and 1.0 V when driving the PXTAL input.

The method and restrictions for varying the frequency on the SA-1100 TXTAL input pin is identical to the preceding paragraph on the PXTAL input pin.

For case number 2 above (where the capacitance prevents the crystals from operating normally), switches S8 and S4 may be thrown to the "dot" position (with S5, S6, S9, and S10 still in the "no dot" position), allowing the PXTAL and TXTAL inputs to be driven by oscillators X4 and X1, respectively. Unfortunately, these oscillators output 5 V CMOS logic levels; therefore, a crude voltage-level-shifting technique is employed with the 74LVC125s and the resistor voltage dividers. While the waveform such a level-shifter produces is not symmetrical, it is periodic and keeps the voltage levels between 0.0 V and 1.0 V.

2.4 Sheet 4 – Memory

The schematic sheet named Memory is a hierarchical partition that contains all components of the SA-1100 microprocessor evaluation platform that are controlled by the signals described in the Memory and PCMCIA Control Module section of the SA-1100 specification.

The three blocks along the left side of this sheet contain all address and control signal fan-out drivers as well as the data buffers present on the SA-1100 microprocessor evaluation platform. Due to the multimoded nature of the SA-1100 microprocessor evaluation platform (which includes two types of boot ROMs, two types of Flash devices, SRAM and DRAM, and so forth), these signals would have been too heavily loaded to be connected directly to the SA-1100.

For a system within the driver-loading specifications of the SA-1100, none of these fan-out buffers or data transceivers will be necessary, except for the signals on the PCMCIA interface. They are needed there because the PCMCIA cards may be hot-inserted or extracted, and these buffers provide the isolation needed so that such activity will not disrupt any other transaction that may be in progress at that moment.

The prefixes for the signals that leave these blocks indicate which section of the memory subsection that they are destined for. The outputs of the `addr_fanout` block electrically re-drive the address signals to the following: `D01_A` signals go to DRAM banks 0 and 1, `D23_A` address signals go to DRAM banks 2 and 3, `S_A` signals go to the SRAM components, `RFR_A` signals go to the ROM and Flash devices, `P0_A` signals go to the PCMCIA bottom slot, and `P1_A` signals go to the top slot of the PCMCIA socket.

The `LA_A` signals go to the logic analyzer connectors on the sheet named `visibility`. Buffering all address, control, and data signals before sending them to the logic analyzer connectors has at least two major advantages on a Design Verification Platform:

1. The logic analyzer connectors may be located in a remote corner of the board without adding length to the traces on the SA-1100 signals.
2. The loading on the SA-1100 signals will be constant, independent of whether the logic analyzer is connected to the system or not.

The four blocks along the right side of the page contain:

- the RAM (SRAM and DRAM)
- the ROMs, Flashes, and a Register (RFR)
- a block for each card slot in the dual PCMCIA socket

The block in the middle, named `Ext_cntl`, contains the "glue" logic (very little of this would be required on any other SA-1100-based system).

2.5 Sheet 5 – Addr_fanout

The schematic sheet named `Addr_fanout` contains the fan-out buffers for the address signals from the SA-1100.

The 74LVC162244 devices have internal 25 Ω series resistors on their outputs. These devices are actually 16-bit wide buffers, but they were drawn as 4-bit wide portions of these devices in order to allow efficient component, gate, and pin wrapping to be performed while the board was in the layout phase of the project.

For a system within the driver loading specifications of the SA-1100, none of these fan-out buffers will be necessary except for the signals on the PCMCIA interface. They are needed there because the PCMCIA cards may be hot-inserted or extracted, and these buffers provide the isolation needed so that such activity will not disrupt any other transaction that may be in progress at that moment.

The buffers that drive the address signals to the two PCMCIA slots are not enabled at all times. The enable signals are generated in the `Ext_cntl` glue logic, and for these buffers to be enabled, the PCMCIA card must already be fully inserted, have power applied (under software control), and have the programmer set a register bit (on the sheet named `Cs3reg`) to allow these drivers to be enabled.

2.6 Sheet 6 – Cntl_fanout

The schematic sheet named Cntl_fanout contains the fan-out buffers for the memory interface control signals from the SA-1100.

The 74LVC162244 devices have internal 25 Ω series resistors on their outputs. These devices are actually 16-bit wide buffers, but they were drawn as 4-bit wide portions of these devices in order to allow efficient component, gate, and pin swapping to be performed while the board was in the layout phase of the project.

For a system within the driver-loading specifications of the SA-1100, none of these fan-out buffers will be necessary except for the signals on the PCMCIA interface. They are needed there because the PCMCIA cards may be hot-inserted or extracted, and these buffers provide the isolation needed so that such activity will not disrupt any other transaction that may be in progress at that moment.

The buffers that drive the control signals to the two PCMCIA slots are not enabled at all times. The enable signals are generated in the Ext_cntl glue logic, and for these buffers to be enabled, the PCMCIA card must already be fully inserted, have power applied (under software control), and have the programmer set a register bit (on the sheet named Cs3reg) to allow these drivers to be enabled.

The resistor pack, RPI, is present so that when an SA-1100 device is not present in its socket, the SA-1100 microprocessor evaluation platform may be powered up and these critical control signals will be held in the inactive state. These signals are used by the CPLDs on the Ext_cntl sheet mainly for data bus transceiver control, and with these signals held inactive, no transceiver contention (fighting) should occur.

2.7 Sheet 7 – Data_buffers

The schematic sheet named Data_buffers contains the data transceivers for the memory interface data bus signals from the SA-1100. Along the left side of the page are buffers connected to the data bus to drive the state of the signals on this bus to the logic analyzer connectors.

The control signals for these transceivers are generated in the CPLDs on the sheet named Ext_cntl.

For a system within the driver-loading specifications of the SA-1100, none of these data transceivers will be necessary except for the signals on the PCMCIA interface. They are needed there because the PCMCIA cards may be hot-inserted or extracted, and these transceivers provide the isolation needed so that such activity will not disrupt any other transaction that may be in progress at that moment.

2.8 Sheet 8 – RAM

The schematic sheet named RAM is a hierarchical partition that contains both the SRAM and DRAM as well as the multiplexer present on the data bus. Since the SA-1100 uses the nCAS[3:0] signals for the byte enables for a SRAM array, both SRAM and DRAM are not supported simultaneously in an SA-1100-based system. While both are physically present on every SA-1100 microprocessor evaluation platform, the user must select which may be used at any given time. The selection mechanism actually controls a multiplexer that determines whether the SRAM or the DRAM is allowed to communicate on the SA-1100's data bus.

2.9 Sheet 9 – RAM_dmux

The schematic sheet named RAM_dmux contains the multiplexer that determines whether the SRAM or the DRAM is allowed to communicate on the SA-1100's data bus. This multiplexer has a very fast propagation delay of under 250 ps. The user makes the selection by using switch S14. In the "dot" position, SRAM is selected; in the "no dot" position, DRAM is selected.

The setting of switch S14 is a control input into the CPLDs on the sheet named Ext_cntl, and this setting may be read by software by reading the register on the sheet named Cs3reg.

2.10 Sheet 10 – SRAM

The schematic sheet named SRAM contains the four asynchronous static RAM devices on the SA-1100 microprocessor evaluation platform. These four Toshiba 128 K x 8-bit SRAMs combine to create 512 KB of SRAM, which is populated across the entire 32-bit data bus. The SRAM devices chosen for the SA-1100 microprocessor evaluation platform project have 15 ns access times, and are not considered to be low power. These relatively fast devices were chosen so that the memory interface of the SA-1100 could be tested, stressed, and verified with a minimum number of wait states (which does not imply zero wait states). Any choice of asynchronous SRAM would be connected the same way that these devices are shown.

2.11 Sheet 11 – DRAM

The schematic sheet named DRAM contains the four banks of Extended Data-Out Dynamic RAM devices on the SA-1100 microprocessor evaluation platform. These eight Toshiba 1 M x 16 bit DRAMs combine to create a total of 16 MB of DRAM, which is 4 MB per bank. The number within the nRAS[x] signal name corresponds to the bank number. The DRAM array is populated across the entire 32-bit data bus. The nCAS[3] signal corresponds to the most significant byte and the nCAS[0] signal controls the least significant byte.

The EDO DRAM devices chosen for the SA-1100 microprocessor evaluation platform project have 60 ns access times, require only a single 3.3 V supply, and support the self-refresh mode of operation to be used when the SA-1100 is in sleep mode.

Note: To put these DRAMs into self-refresh mode, both the nRAS[x] and the nCAS[x] input signals are asserted low by the SA-1100. Consider this when deciding whether to enable the data bus transceivers on a byte-lane basis based on the assertion of the four nCAS[3:0] signals.

2.12 Sheet 12 – Rfr

The schematic sheet named Rfr is a hierarchical partition that contains the schematic blocks for two possible boot ROMs, two possible Flash implementations, and an external 32-bit register that is addressed with the static chip-select signal nCS[3].

2.13 Sheet 13 – ROM

The schematic sheet named ROM shows the default boot ROM implementation that will be present on every SA-1100 microprocessor evaluation platform initially. The boot ROM devices are actually Flash memory components with their WE# input control signals pulled up (inactive). They reside in the SA-1100's nCS[0] address space.

The devices chosen are the Atmel AT29LV1024 -15JC devices. These devices meet the following criteria:

- The same devices are to be used for boot ROM and Flash memory to reduce the number of devices that had to be ordered and kept in inventory.
- They had to be socketed.
- The SA-1100's ability to correctly access 32-bit wide and 16-bit wide boot ROM implementations had to be tested,
- It needed to be a very low-power device.

The Atmel device, being a 3.3 V-only device is with a 16-bit wide data port in a PLCC-44 package and a power dissipation of just 54 mW.

The selection of whether the SA-1100 accesses the boot ROM with 16-bit wide data or 32-bit wide data is user selected by switch S15, which controls the state of the ROM_SEL input to the SA-1100. The SA-1100 samples the level of this input signal immediately when coming out of the Reset state. When S15 is in the "dot" position, ROM_SEL is high and data is accessed 32 bits at a time from both U35 and U45. When S15 is in the "no dot" position, ROM_SEL is low and data is accessed only from the least significant half of the data bus (U45).

The ROM_SEL signal also is used to control the proper connectivity of the address lines to the boot ROM when in these two modes. When accessing boot ROM data 32 bits at a time, address signal RFR_A[2] is the least significant address bit presented to both U35 and U45. When accessing boot ROM data 16 bits at a time, address signal RFR_A[1] is the least significant address bit presented to U45 (and the unused U35). U35 does not have to be removed when operating this boot ROM in 16-bit wide mode.

2.14 Sheet 14 – ROM2

The schematic sheet named ROM2 shows the socket that allows for a second boot ROM implementation on the SA-1100 microprocessor evaluation platform. When installing a SIMM-type daughtercard into this connector, both U35 and U45 must be removed from their sockets. This connector allows users with different boot ROM criteria than the ones described in the sheet named ROM to design a simple daughtercard that can be populated with devices that meet their criteria. There is no address shifting or multiplexing present on the SA-1100 microprocessor evaluation platform for this socket, so the designer of the daughtercard must connect the address signals according to the width of the data bus that is populated on the daughtercard.

This JAE socket is addressed by the SA-1100's nCS[0] signal. In addition, pin 7 has a signal named ROM2IO_CE# that is created by a CPLD on the sheet named Ext_cntl, is mapped to the SA-1100's nCS[2] signal, and may be used for writing to this boot ROM while in the SA-1100 microprocessor evaluation platform system.

There should be adequate pins allocated for +3.3 V and GND, with 5 V and 12 V both present on single pins as well. All power pins also have a decoupling capacitor.

2.15 Sheet 15 – Flash

The schematic sheet named Flash shows the default Flash memory implementation that will be present on every SA-1100 microprocessor evaluation platform initially. These are the same Flash memory devices that are used for the default boot ROM on the SA-1100 microprocessor evaluation platform.

In addition to the criteria that were listed for the sheet named ROM, the Flash devices needed to operate from a single 3.3 V supply. The devices used are the Atmel AT29LV1024-15JC devices.

The selection of whether the SA-1100 accesses the Flash memory with 16-bit wide data or 32-bit wide data is user selected by switch S13, from which the programmer can read the state of the least significant bit (F32/16#) of the register found on the sheet named Cs3reg. This register bit should be interrogated by software before configuring the SA-1100's memory interface control registers that control the nCS[1] signal.

When S13 is in the "dot" position, F32/16# is high and data is accessed 32 bits at a time from both U34 and U44. When S13 is in the "no dot" position, F32/16# is low and data is accessed only from the least significant half of the data bus (U44).

The F32/16# signal also is used to control the proper connectivity of the address lines to the Flash memory devices when in these two modes. When accessing data from Flash memory 32 bits at a time, address signal RFR_A[2] is the least significant address bit presented to both U34 and U44. When accessing data to/from Flash memory 16 bits at a time, address signal RFR_A[1] is the least significant address bit presented to U44 (and the unused U34). U34 does not have to be removed when operating this Flash memory in 16-bit wide mode.

2.16 Sheet 16 – Flash2

The schematic sheet named Flash2 shows a second Flash memory implementation that could be present on any SA-1100 microprocessor evaluation platform. The two devices shown, U33 and U43, are manufactured by Sharp. They have a higher density and faster access time than the default Flash memory Atmel devices. They also require two voltage sources.

The SA-1100 microprocessor evaluation platform has the surface-mount land patterns for these two devices, but they are unpopulated unless the end user acquires these devices and solders them down. If this is done, the default Flash memory devices U34 and U44 must be removed from their sockets.

2.17 Sheet 17 – Cs3reg

The schematic sheet named Cs3reg shows a 32-bit register that the programmer accesses by any read or write that is mapped to the SA-1100's nCS[3] signal. Also present are two 12 V, 30 mA supplies (Linear Technology LTC1262CS8s) for the PCMCIA VPP inputs, and a Maxim* MAX1600EAI power switch, all of which are directly controlled by the programmer manipulating bits in this register.

The cs3reg is 32 bits wide, and is redundantly mapped to every word in the SA-1100's nCS[3] space. The most significant 16 bits are read/write, while the least significant bits of this register are read-only.

Reading bits cs3reg[7:5] always return a binary value of 0b001, which is intended to signify that this is a SA-1100 microprocessor evaluation platform system. Bits cs3reg[4:0] allow the programmer to read the state of five switch settings that the user has manually configured for the SA-1100 microprocessor evaluation platform.

Writes to the most significant byte of the register, cs3reg[31:24], effect the operation of the PCMCIA card inserted into the top socket of the two-card cage. These signals have the P1_ prefix on their names. Writes to the next most significant byte of the register, cs3reg[23:16], effect the operation of the PCMCIA card inserted into the bottom socket of the two-card cage. These signals have the P0_ prefix on their names.

The P1_SW_RST# and P0_SW_RST# signals (cs3reg[31] and cs3reg[23], respectively) allow the programmer to independently assert and deassert the reset signals to the two PCMCIA cards. The P1_DRVEN and P0_DRVEN signals (cs3reg[30] and cs3reg[22], respectively) allow the programmer to independently enable the fan-out drivers and data transceivers for each card (shown on sheets 5, 6, and 7).

All bits in the 16-bit writable (most significant) portion of the cs3reg are cleared to zero whenever the SA-1100 microprocessor evaluation platform is reset (by U47 or S16 on sheet 30 - Input_pwr).

While not shown on this schematic sheet, it is important to note that whenever the two PCMCIA cards are inserted or ejected, software will be notified immediately by a transition on the GPIO[4] and GPIO[7] pins of the SA-1100. Whenever the bottom PCMCIA card (P0) is inserted, there will be a falling edge on the GPIO[4] pin, and there will be a rising edge on that pin whenever that PCMCIA card is ejected. The same relationship exists with the top PCMCIA card (P1) and the SA-1100's GPIO[7] pin.

Upon software being notified that a PCMCIA card has been fully inserted (by a falling edge on GPIO[4] or GPIO[7]), bits cs3reg[13:12] or cs3reg[9:8], respectively, should be read to determine the initial voltage to be applied to the V_{CC} pins for that PCMCIA card. Writing a one to cs3reg[28] and/or cs3reg[20] will enable (turn on) the 12 V supply for the PCMCIA card. Writing to cs3reg[27:24] will select the voltage levels supplied to the V_{CC} and V_{PP} pins for the top PCMCIA card (P1), and writing to cs3reg[19:16] will do the same to the bottom PCMCIA card (P0).

The programmer is referred to the MAX1600EAI data sheet for the appropriate encodings (the input pin named CODE is tied to ground on the SA-1100 microprocessor evaluation platform). Once the proper voltage levels have been applied to the PCMCIA card, and after the appropriate time delay (a software loop > 300 ms), cs3reg[30] and/or cs3reg[22] should have ones written to them (to enable the address and control fan-out buffers) at the same time that a one is written to cs3reg[31] and/or cs3reg[23], which will deassert the RESET# signal to the PCMCIA card. The RESET# signal must be deasserted for a minimum of 10 μ s. In addition, the programmer must wait a minimum of 20 ms from the time that RESET# is deasserted before any accesses to the PCMCIA card are performed.

When a PCMCIA card is ejected, there will be a rising edge on GPIO[4] or GPIO[7], and hardware will automatically disable the address and control signal fan-out buffers for that slot. Hardware will also automatically assert the RESET# signal to the appropriate slot. Software should then write all zeros to cs3reg[31:24] or cs3reg[23:16], depending on which PCMCIA card was ejected, to turn off all voltage sources to that slot and to ensure that the RESET# signal will be asserted when the user re-inserts a card into that slot.

2.18 Sheet 18 – PCMCIA0

The schematic sheet named PCMCIA0 shows the connections to the bottom slot of the two-slot PCMCIA socket. The 74LVC125 buffer/gates serve the purpose of voltage-level shifting from the potentially 5 V PCMCIA signal levels down to the 3.3 V levels for the SA-1100 and the CoolRunner CPLDs, both of which do not have 5 V tolerant inputs. (Note that the 74LVC125 is 5 V tolerant, but that the 74LVC162244 is not.)

Switch S12 is utilized on the SA-1100 microprocessor evaluation platform so that the user may select whether GPIO[7:2] are to be used for PCMCIA signals or whether they are to be used by the SA-1100 for driving a 16-bit color LCD panel. The SA-1100 microprocessor evaluation platform always allows simultaneous operation of an 8-bit (color or mono) LCD panel with the dual PCMCIA cards. The mutually exclusive relationship between 16-bit color LCD and PCMCIA operation is a limitation of the SA-1100 microprocessor evaluation platform system, and can easily be avoided by any system design that would utilize a different set of SA-1100 GPIO pins for the PCMCIA functionality.

Note that GPIO[4] is used to detect when the bottom PCMCIA card (P0) is fully inserted into its socket (both P0_CD1# and P0_CD2# are low). GPIO[3] is used as the interrupt request signal from this PCMCIA card, and GPIO[2] is used to monitor the transitions of the P0_STSCHG# signal. Also notice that the input signal to this buffer, P0_SW_STSCHG#, can be read at cs3reg[10] for operating systems that poll the state of this signal rather than have the transitions cause interrupts.

2.19 Sheet 19 – PCMCIA1

The schematic sheet named PCMCIA1 shows the connections to the top slot of the two-slot PCMCIA socket.

Switch S12 on the PCMCIA0 sheet also controls the 74LVC125s found on the PCMCIA1 sheet.

Note that GPIO[7] is used to detect when the top PCMCIA card (P1) is fully inserted into its socket (both P1_CD1# and P1_CD2# are low). GPIO[6] is used as the interrupt request signal from this PCMCIA card, and GPIO[5] is used to monitor the transitions of the P1_STSCHG# signal. Also notice that the input signal to this buffer, P1_SW_STSCHG#, can be read at cs3reg[14] for operating systems that poll the state of this signal rather than have the transitions cause interrupts.

The 74LVC86 exclusive-OR gate, U17B, is used to combine the pulse-width-modulated speaker outputs of the two PCMCIA cards. The output of this gate is routed to a buffer on sheet 27, named CODECs, and then is connected to a test point where the user may attach an actual speaker.

2.20 Sheet 20 – Ext_cntl

The schematic sheet named Ext_cntl shows the two CoolRunner CPLDs used on the SA-1100 microprocessor evaluation platform. The functionality was partitioned so that one CPLD controlled the memory array logic while the second was dedicated to the PCMCIA control. The source equations for both of these CPLDs are found in the files named MEMCNTL.PHD and PCMCIA.PHD, both of which may be opened with any standard ASCII text editor such as vi, emacs, NotePad, or SimpleText.

There are no clocks going into either of these CPLDs, and all outputs are created by simple Boolean combinatorial logic from the inputs. The functionality contained within these two CPLDs may or may not be required in another SA-1100-based system.

The MEMCNTL CPLD is used on the SA-1100 microprocessor evaluation platform for data bus transceiver control, generating SRAM chip-enables, and cs3reg read and write control signals. This CPLD monitors the state of two user-selectable switches, S11 and S14. Switch S11 is used to determine whether the SA-1100's nCS2 signal is to be used for SRAM chip enables or for writes to boot ROM (writes to ROM2 occur in nCS2 space). Switch S14 is configured by the user to select whether the SA-1100 microprocessor evaluation platform is to operate with either SRAM or DRAM. (Both are physically present on the SA-1100 microprocessor evaluation platform, but only one may be used on any given run.)

The PCMCIA CPLD is used on the SA-1100 microprocessor evaluation platform for PCMCIA address and control signal fan-out buffer output enable control, PCMCIA data transceiver control, and combining the WAIT# and IOIS16# signals from the two PCMCIA cards for the single input into the SA-1100.

The remaining buffers on this schematic sheet are used to redrive an abundance of signals to the logic analyzer connectors. These signals are mainly of interest to the SA-1100 microprocessor evaluation platform board bring-up team.

2.21 Sheet 21 – Peripherals

The schematic sheet named Peripherals is a hierarchical partition that contains all components of the SA-1100 microprocessor evaluation platform system that are controlled by the signals described in the LCD Controller and Serial Port 1 through Serial Port 4 sections of the SA-1100 specification. This schematic sheet corresponds directly with the block named peripherals on the topmost schematic sheet named Brutus.

The four blocks named Serials, LCDs, CODECs, and Alt_functs contain the circuitry that the designer of an SA-1100-based system would be interested in examining. Designers could easily extract and copy the portions that apply to their set of design goals. If the SA-1100 microprocessor evaluation platform does not offer a "perfect solution" to the design goals of the peripherals required in the designer's system, then it is hoped that the SA-1100 microprocessor evaluation platform schematics can be used as a "starting point" upon which any number of modifications could be implemented.

The two blocks named GPIO_vis and Periph_vis contain the buffers to redrive the GPIO signals, the LCD control signals, and the serial port signals out to the logic analyzer connectors. In addition, the LCD control signals are fanned-out here.

2.22 Sheet 22 – GPIO_vis

The schematic sheet named GPIO_vis contains two types of buffers. The standard 74LVC162244 devices used throughout the rest of the SA-1100 microprocessor evaluation platform system are used to buffer and send the state of all of the SA-1100 GPIO signals out to the logic analyzer connectors.

A second type of buffer, the Toshiba TC74VHCT244AF, is used to create a set of LCD signals that have the CL_ prefix added to their name. They were named this way because they are used to drive the color LCDs chosen to operate with the SA-1100 microprocessor evaluation platform. It would be more appropriate to think of the CL_ prefix as CMOS levels. This Toshiba device was chosen because its data sheet states that it has a V_{OH} minimum of 3.94 V, with an I_{oh} of -8 mA. These parameters are necessary because both of the color LCDs chosen to operate with the SA-1100

microprocessor evaluation platform have a V_{ih} minimum specification of $V_{CC} \times 0.8$. While this Toshiba device does not meet this specification under worst-case conditions, it is the best device for this application.

2.23 Sheet 23 – Periph_vis

The schematic sheet named Periph_vis also contains the two types of buffers found on the previous sheet (named GPIO_vis).

Most of the buffers on this schematic redrive the SA-1100 signals from the serial ports and the LCD controller out to the logic analyzer connectors.

The LCD signals that have the ML_ prefix were named this way because they are used to drive the mono LCDs. Both of the mono LCDs chosen to operate with the SA-1100 microprocessor evaluation platform require only TTL signal levels; therefore, these signals would have been more appropriately named with a TL_ prefix. The 74LVC162244 outputs 3.3 V TTL voltage levels, so these devices are used to drive the LCD control signals to the two mono LCD connectors on the SA-1100 microprocessor evaluation platform.

2.24 Sheet 24 – Alt_funcs

The schematic sheet named Alt_funcs contains the keyboard controller, two debounced switches, and a few discrete LEDs.

The keyboard controller used is manufactured by USAR Systems. On the SA-1100 microprocessor evaluation platform, it attaches to the SA-1100 using GPIO[13:10], which are the "alternate function" pins for serial port 4's SSP using a subset of the Motorola SPI protocol. Switch S20 allows the user to simulate the sensor used to report when the system's lid is open or closed. Switch S19 is intended by the UR5HCSPI-06-FB to be an external switch: one that can be manipulated by the user even when the lid is closed. The discrete LED, D16, is turned on and off by the programmer manipulating the registers internal to the keyboard controller. This LED may be thought of as the equivalent of a "Caps Lock" light, or may be used by the programmer to verify that the keyboard controller is correctly being communicated with.

This keyboard controller will operate only with the Fujitsu FKB1406 keyboard. Although the two connectors on the SA-1100 microprocessor evaluation platform have 17 pins and 10 pins, the flex cable from the Fujitsu keyboard has only 14 and 7 contacts, respectively. When inserting the flex cables from the keyboard into the connectors on the SA-1100 microprocessor evaluation platform, it is important that the unused connector pins are "on the outside" of both connectors.

The two switches, S21 and S22, are debounced by U57 and they directly control the state of the SA-1100's GPIO[1:0] pins. These two GPIO pins are special because transitions on either of these two pins can be potential wake-up sources when the SA-1100 is in sleep mode.

The three discrete LEDs, D3, D4, and D17, can be used for any purpose that the programmer wishes. Note that when the SA-1100 is operating in 16-bit LCD mode, D3 and D4 probably will be changing state continuously.

2.25 Sheet 25 – Serials

The schematic sheet named Serials contains the serial ports that allow the transfer of information between the SA-1100 microprocessor evaluation platform and another computer. Included are an AppleTalk,* GeoPort,* a USB slave, IrDA, and two standard DTE-to-DTE serial ports.

The AppleTalk port is connected to the SA-1100's serial port 1 SDLC controller via the TXD_1 and RXD_1 pins. In addition, GPIO[17:16] are used in their alternate function mode, as listed in Section 9.1.2 of Rev. 2.0 of the SA-1100 Data Sheet. GPIO[19:18] have been used as handshaking inputs to the SA-1100. These two signals as well as the RXD_1 signals to the SA-1100 had the voltage level shifted down to 3.3 V TTL by the 74LVC125s. The combination of 51-ohm resistors and 100-pF capacitors on each signal going to the Mini-DIN-8 connector are recommended by Linear Technology Corporation, who manufactured the AppleTalk transceiver LTC1323CG for EMI control when used in an actual production system (which the SA-1100 microprocessor evaluation platform is not).

The IrDA transceiver, D6, is manufactured by Temic. It is connected to the SA-1100's serial port 2. The RXD_2 input to the SA-1100 has had the voltage level shifted down to 3.3 V TTL by the 74LVC125. This transceiver comes up from RESET# in the 115-kb/s mode, but can be put into the 4 Mb/s mode by transitioning the SD pin as described in the data sheet for the TFDS6000 device. The three 18-ohm resistors in parallel result in a 6-ohm resistor of sufficient power dissipation to handle the transmitter LED with a maximum on-time duty cycle of 25%.

The two DB9_male connectors allow DTE-to-DTE communication only (i.e., can not connect a modem). Connector J23 allows communication to the SA-1100's serial port 3, while connector J22 communicates to the SA-1100 via the GPIO[15:14] pins, which are the alternate function pins for serial port 1's UART. These are not full RS-232 implementations, because only the RXD and TXD signals are present on the connectors; the CTS, DTR, RTS, and so forth are not present. The system designer who desires to implement the full RS-232 protocol can easily do so by assigning these handshake signals to SA-1100 GPIO pins of their choice. The Maxim MAX3223 transceiver uses 3.3 V as its supply voltage, and so the signals that it sends back to the SA-1100 do not need to be level shifted down from 5 V.

Connector J20 is a type-B universal serial bus (USB) connector, which is the type of USB connector present on a slave device. The SA-1100 is never a USB master or hub controller. The only requirement for all SA-1100-based systems with a USB port is to include a 22-Ohm resistor physically next to the SA-1100's UDC+ and UDC- pins. These resistors are shown as R241 and R242 on the serials schematic. The device D8, which is a Microsemi USB0805C data line voltage suppressor, is an excellent example for effective ESD protection. This device will work in conjunction with the two 22 Ω resistors to protect the SA-1100 from ESD on the USB port. Because there is no USB transceiver (such as on the AppleTalk and serial ports), the SA-1100 is connected directly to the USB connector and cable (with only the 22 Ω -resistors as isolation). Therefore, it is highly recommended that every SA-1100-based system with a USB port implement some type of ESD protection scheme.

The SA-1100 microprocessor evaluation platform connects a 1.5 K Ω resistor, R261, as a pull-up on the D+ line, which effectively tells the master or hub on the other end of the USB cable that it is to communicate at the 12 Mb/s rate. The 3.3 V that this pull-up resistor is connected to is created from the +5 V that is provided from the master or hub via the USB cable. This is accomplished using the Texas Instruments TPS7133QPW low-drop-out (LDO) voltage regulator. This voltage regulator is enabled only when the USB cable is properly connected to an upstream device (master or hub) and when the SA-1100 is not in sleep mode. By doing so, the upstream device will not see the D+ signal pulled up at that time and will think that the SA-1100 microprocessor evaluation platform is not connected to the USB cable; therefore, it will not attempt to communicate to the SA-1100 microprocessor evaluation platform when the SA-1100 is in sleep mode.

2.26 Sheet 26 – LCDs

The schematic sheet named LCDs contains the connectors for multiple LCD panels, although only one LCD panel should be connected at any one time.

The connectors J2 and J5 are used specifically to interface with a Sharp LM5H40TA mono LCD panel, but this particular panel is an emerging technology, and the SA-1100 was never specified to support such an LCD. The connectors remain on this schematic sheet because this incompatibility was not discovered until the SA-1100 microprocessor evaluation platform printed circuit board was in the physical design stage. A future revision of the SA-1100 may support this panel.

Connector J4 allows the connection to a small mono LCD that is to be used on a Intel internal SA-1100-based R&D project.

Connectors J27 and J6 are the two connectors that will be used by virtually all SA-1100 microprocessor evaluation platform systems sent out. J27 is for connecting a Kyocera KCS3224ASTT-X1, which is a 320 x 240 pixel 8-bit color STN LCD with a 5.7-inch diagonal viewing area. Connector J6 interfaces to the Hitachi PH-BLC08-K2 inverter for the backlight on the Kyocera LCD. Voltage measurement on test point TP3 should ensure that the voltage is between +9 V and +19 V (adjustable by R4 found on the schematic sheet named Lcd_pwr) before turning off the power to the SA-1100 microprocessor evaluation platform and then connecting the cable to the Hitachi inverter. Once connected, and poweredup, R5 may be adjusted to achieve the best backlight illumination.

Connectors J1 and J7 are for support of a TFT color LCD panel. Only two of these expensive Sharp LCD panels have been used in the lab. This is for the explicit purpose of verifying that the SA-1100 can correctly operate with such an LCD panel. Support for this panel is minimal. The voltages required by the inverter are not present on the SA-1100 microprocessor evaluation platform, and must be applied by attaching external power supplies to the test points TP4-7 and TP15. It is not possible to operate the SA-1100 microprocessor evaluation platform with this LCD and the PCMCIA cards simultaneously. The user must select one of these two mutually exclusive modes (for the SA-1100 microprocessor evaluation platform) by setting switch S12 as shown on the sheet named PCMCIA0.

When operating the SA-1100 microprocessor evaluation platform with either of the two color LCDs, switch S1 must be in the "dot" position for two important reasons. First, the position for this switch is readable by the programmer by reading cs3reg[4]. This indicates which mode the SA-1100 LCD controller should be configured for. Although there are two possible color LCDs that can be connected to the SA-1100 microprocessor evaluation platform, when the switch is set to a one indicating a color LCD panel, software should assume that the 8-bit color Kyocera is the one actually connected to the SA-1100 microprocessor evaluation platform. The second reason that switch S1 must be set correctly is that only the color LCDs have inverters for their backlights. The switch S1 is connected to the enable input for the converter on the SA-1100 microprocessor evaluation platform which creates the required voltage for the inverters. With this switch set to a low, or zero, the converter will be disabled, and the backlight will be unable to operate.

Also on this page is switch S2, which is the more conventional method of turning the LCD backlight on and off. This switch should be set to the "no dot" position to have the backlight turned on.

2.27 Sheet 27 – CODECs

The schematic sheet named CODECs contains two different analog front-end devices, only one of which should be soldered to the SA-1100 microprocessor evaluation platform at any one time. CODEC is an acronym for COmpression/DECompression. These two devices are connected to the SA-1100's serial port 4 multimedia communications port controller using the pins SCLK_C, TXD_C, RXD_C, and SFRM_C. In addition, the SA-1100 pin GPIO[22] has been used on the SA-1100 microprocessor evaluation platform for the interrupt request from the CODECs.

The top device, U46, is manufactured by Philips Semiconductor, and is known as the UCB1100. The bottom device, U55, is manufactured by Cirrus Logic, and is known as the CS4271. The Philips device is being replaced by the pin-for-pin compatible UCB1200, which is supposed to be greatly enhanced over the UCB1100, but was not available at the time the SA-1100 microprocessor evaluation platform was designed and built. Although these two devices perform the same functions, they come in two different packages with two different pin-outs. Therefore, the SA-1100 microprocessor evaluation platform has simply connected both devices in parallel on the printed circuit board but only one footprint may actually have a device soldered to it at any given time. These devices are located at the front-left corner of the SA-1100 microprocessor evaluation platform where no other digital signals are routed. About half of the SA-1100 microprocessor evaluation platform systems will contain the UCB1100, while the other half will contain the CS4271 (and five boards will be built with some initial samples of the UCB1200).

These devices are intended to directly interface to a resistive touchscreen. The SA-1100 microprocessor evaluation platform uses the DynaPro #95638 because it is big enough to fit over all four of the LCDs that were designed to connect to SA-1100 microprocessor evaluation platform. It is not known whether the capacitors C203-C206 are actually needed. Connector J3 is a simple 4-pin right-angle stake pin arrangement.

In addition, the CODEC device will interface directly to a microphone and speaker, both of which are included on every SA-1100 microprocessor evaluation platform system. These devices currently support only monaural audio; stereo is not yet available.

Test points TP88, TP89, TP85, and TP90 are connected to the four analog-to-digital inputs on the CODECs. If the user wishes to connect an analog device to these test points, then test points TP83 and/or TP84 should be used as the analog ground when the SA-1100 microprocessor evaluation platform system contains a UCB1100. Likewise, test points TP87 and/or TP91 should be used as the analog ground when the SA-1100 microprocessor evaluation platform system contains a CS4271. Trim-pot R21 can be used to emulate components such as a battery voltage monitor.

Daughtercard DC1 is known as a DAA, and its purpose is to match the impedance to the telephone line and to provide isolation of SA-1100 microprocessor evaluation platform SA-1100 microprocessor evaluation platform from the telephone system. The device installed on the SA-1100 microprocessor evaluation platform is manufactured by Xecom and passes all regulatory testing in North America and Japan. Xecom makes DAAs that can be used worldwide, but the XE0071 used on the SA-1100 microprocessor evaluation platform is small in size, has a reasonable cost, and should work in Europe, too; however, it is not certified to meet the higher isolation voltages required there.

There are several discrete resistors and capacitors on the SA-1100 microprocessor evaluation platform that are between the CODECs and the DAA. The actual values chosen are a compromise between the values listed in the data sheet specifications for the two CODECs and the DAA. The DAA is connected to the two central conductors of the RJ11 telephone jack.



The CODEC devices also have 10 general-purpose I/O pins, much like the GPIO[27:0] pins on the SA-1100 (a transition can cause an interrupt). Two of these general-purpose I/O pins on the CODECs have been used to interface to the DAA off-hook (DAA_OH) and ring-indicator# (DA_RI#) pins.

Six of these CODEC general-purpose I/O pins are used to drive LEDs that can be used for any purpose that the programmer wishes. IO[6] will turn on the red LED, D9, when it is driven low. IO[5] will turn on the green LED, D10, when it is driven low. To provide additional flexibility, a seven-segment LED, with a built-in decoder, has been connected to IO[3:0].



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