



Intel[®] StrongARM[®] SA-1111 Development Module

Schematics

Advance Information

February 2000

Phase 4

Notice: This document contains information on products in the sampling and initial production phases of development. Revised information will be published when this product is available.

Order No: 278282-004



Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

The SA-1110 Development Module may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Copyright © Intel Corporation, February 2000

*Other brands and names are the property of their respective owners.

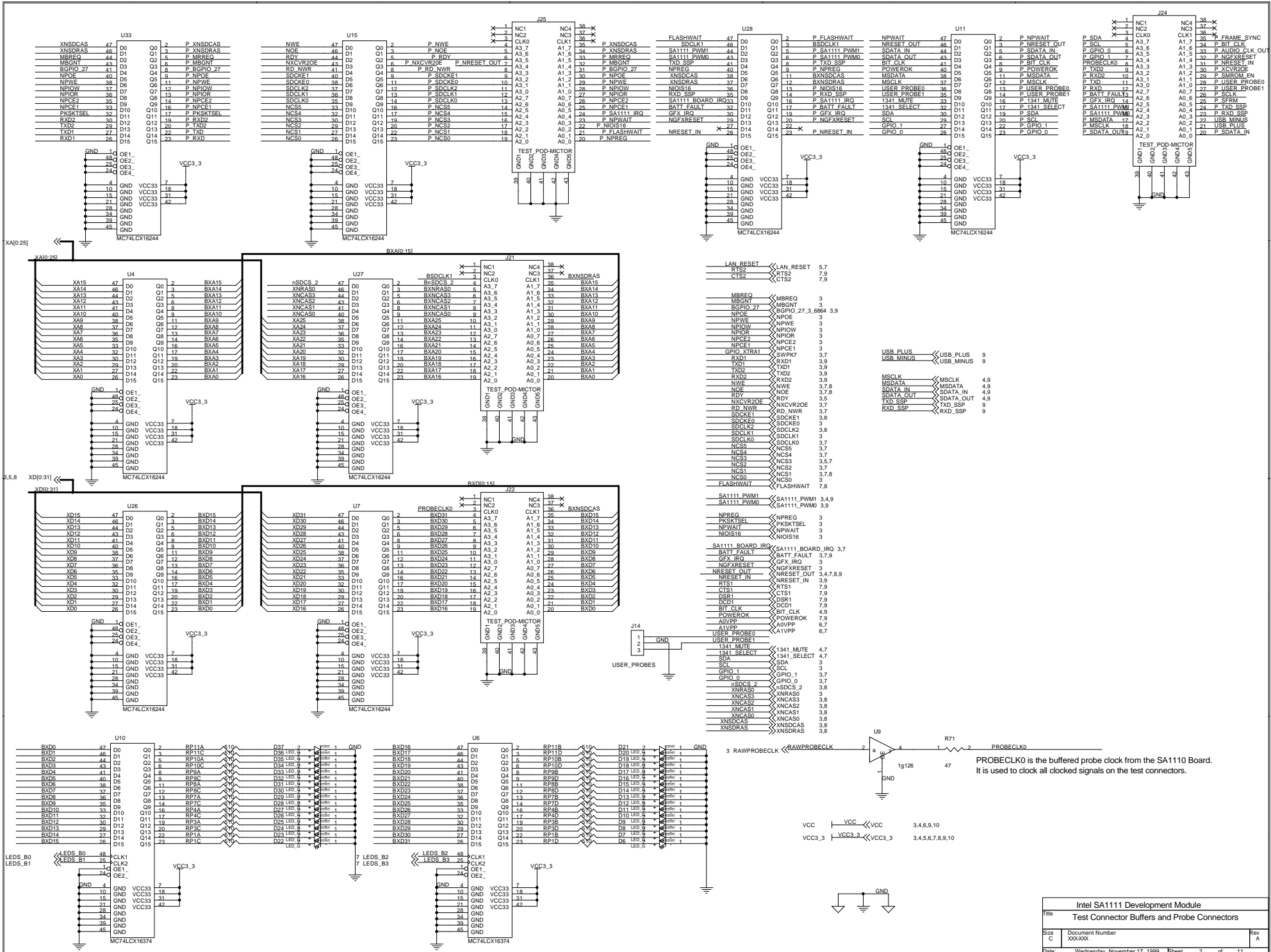
ARM and StrongARM are registered trademarks of ARM, Ltd.

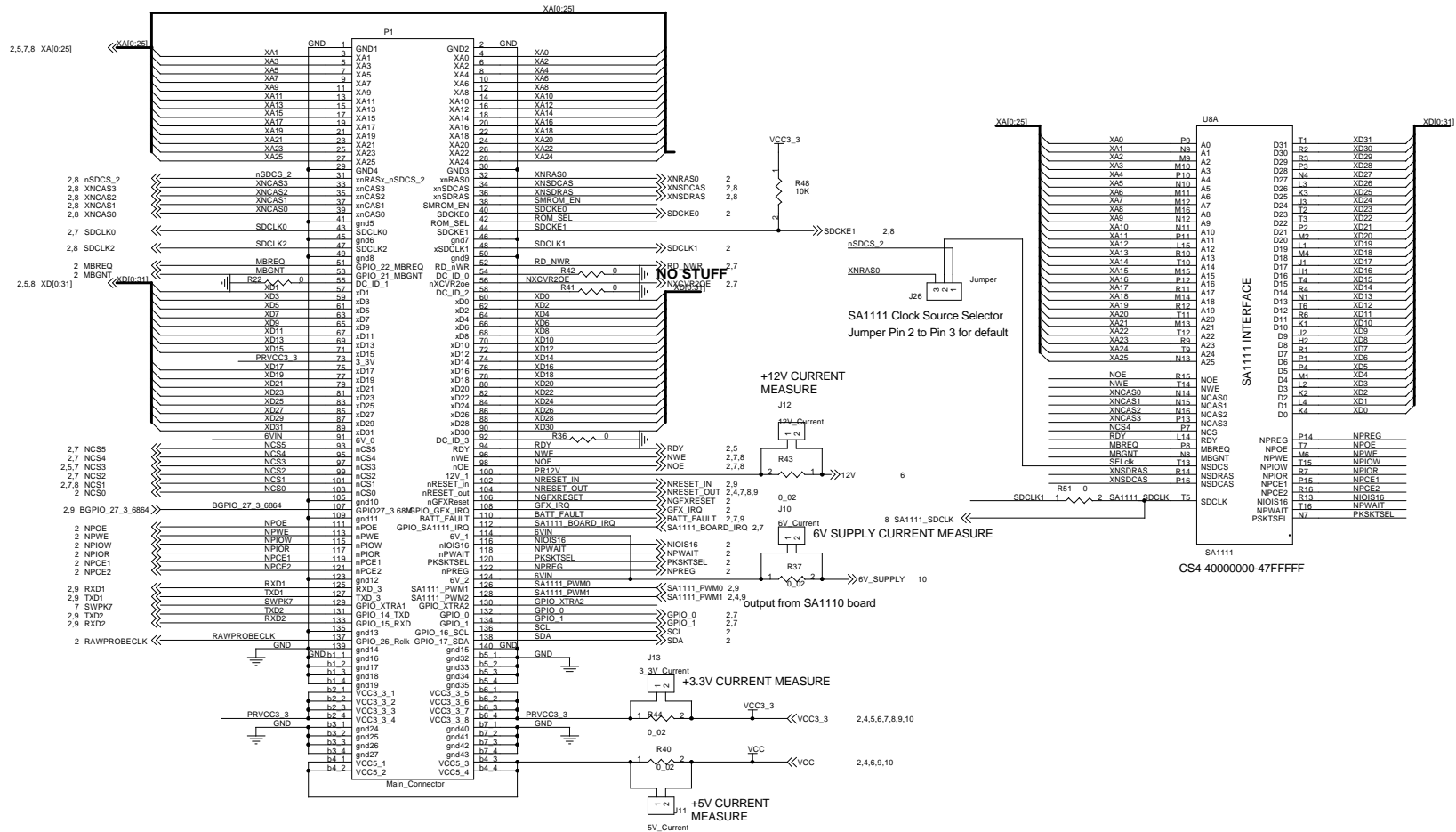


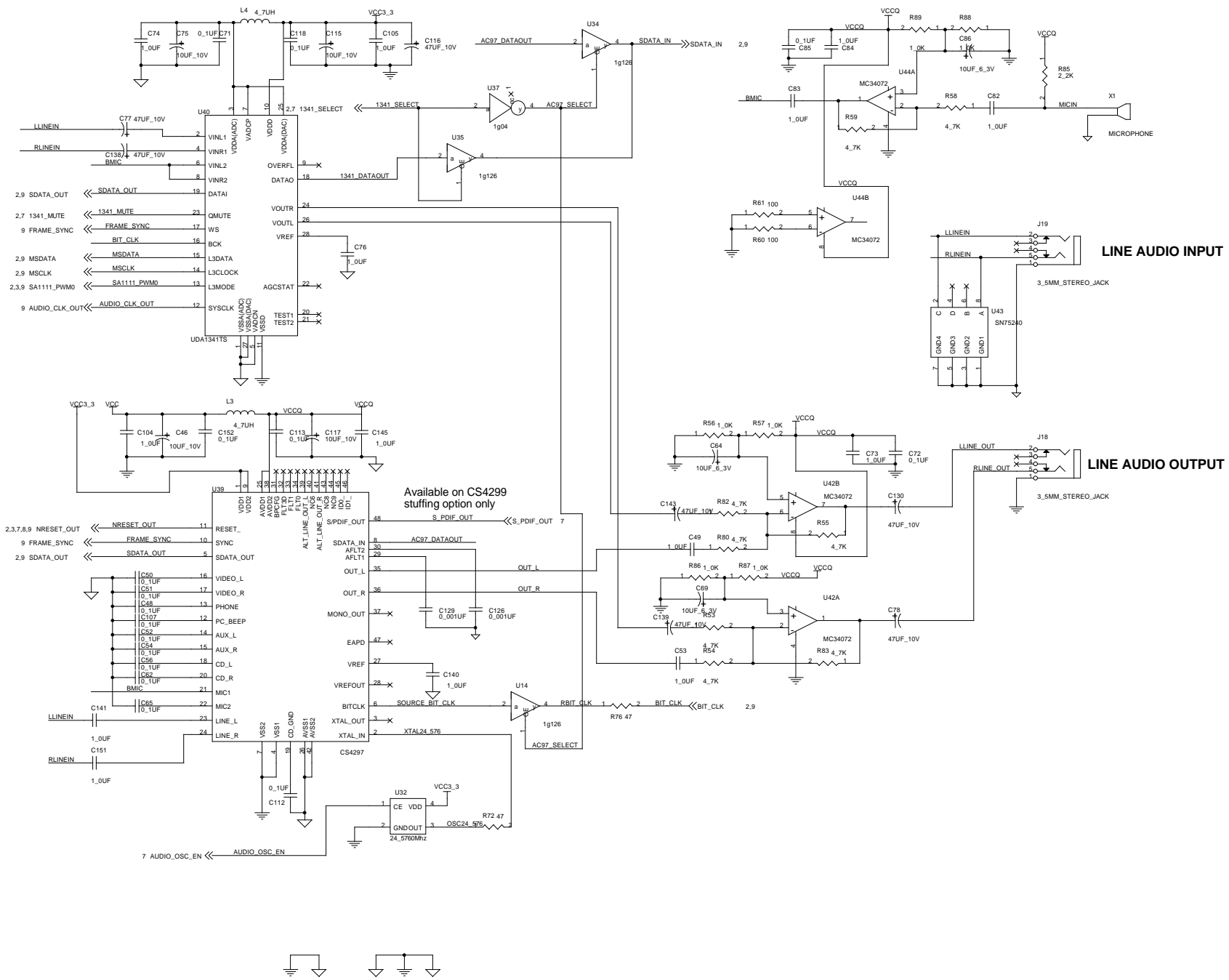
1.0 SA-1111 Development Module Schematics

This document contains the electrical schematics and revision information for the Intel® StrongARM® SA-1111 Development Module (SA-1111 Development Module).

Note: This document and module are for the Phase 4 hardware build of this product. For the latest information and updates, see the hardware release notes that are provided in hardcopy format, and the software readme.txt files that are provided in the software kits.
Sheet 11 of 11 has been omitted because it contains historical information.

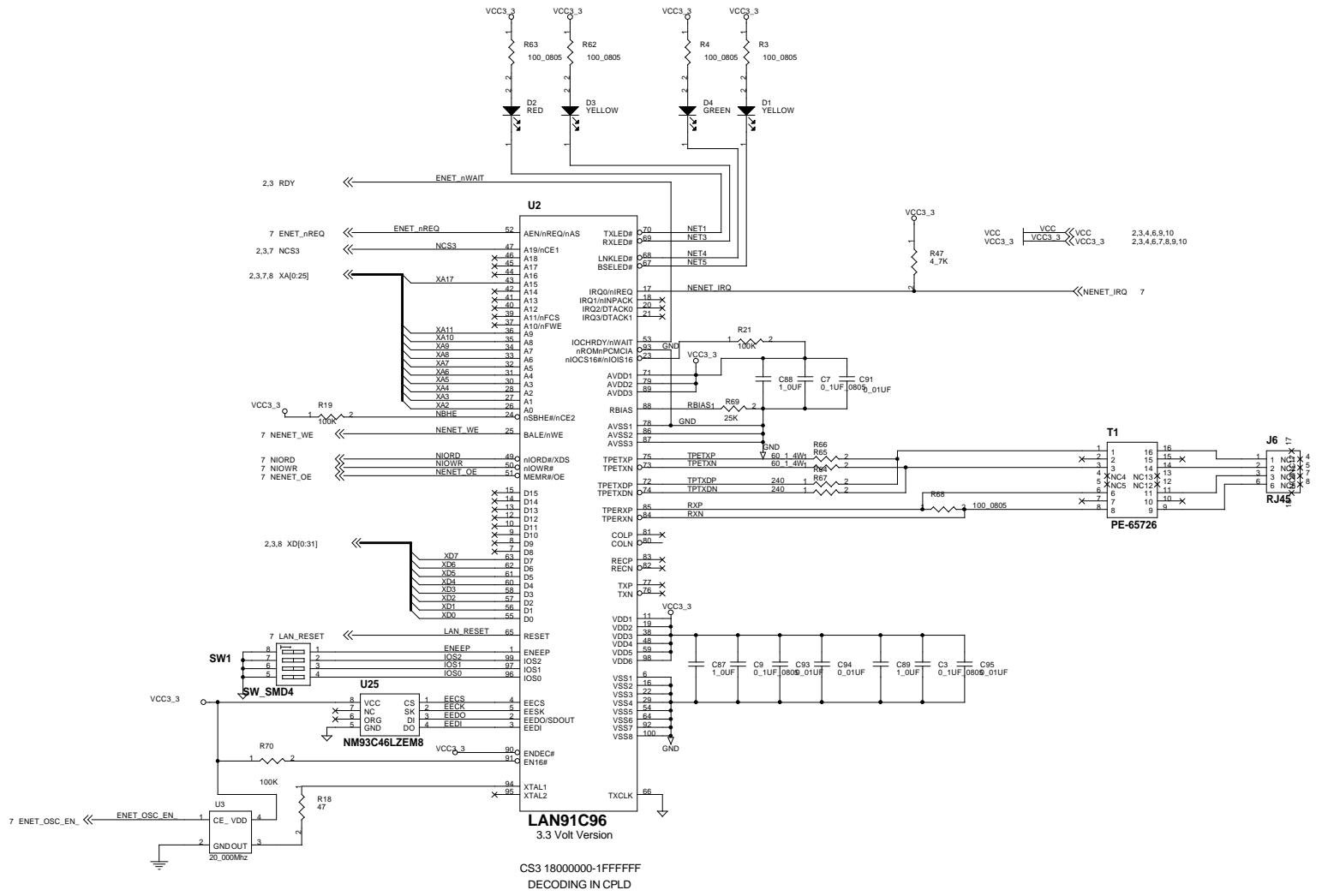




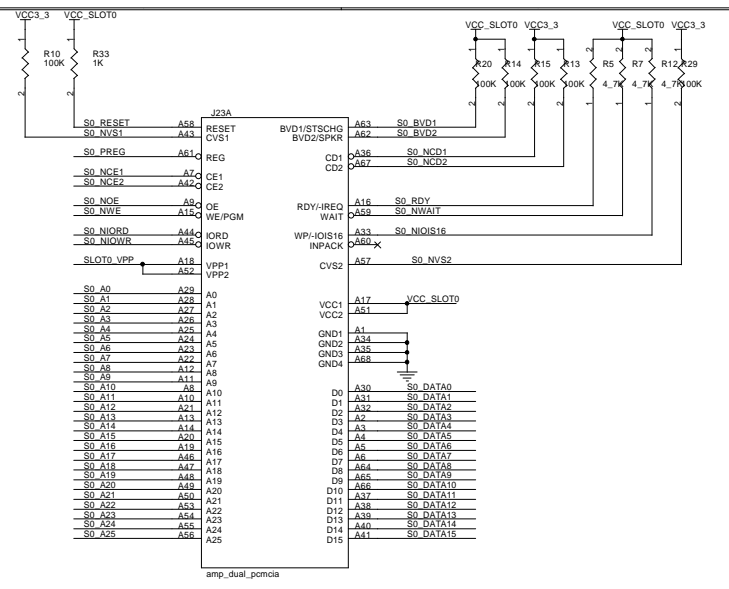


VCC VCC VCC
 VCC3_3 VCC3_3 VCC3_3
 2.3.6.9.10
 2.3.5.6.7.8.9.10

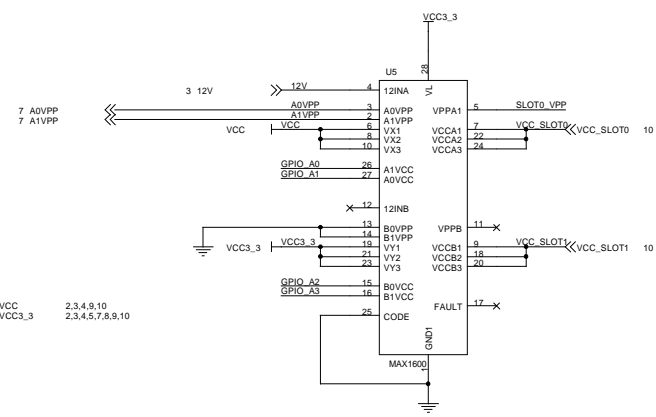
Intel SA1111 Development Module			
AUDIO Components			
File	Document Number		
Size	XXXXXX		
C	Rev A		
Date:	Wednesday, November 17, 1999	Sheet	4 of 11



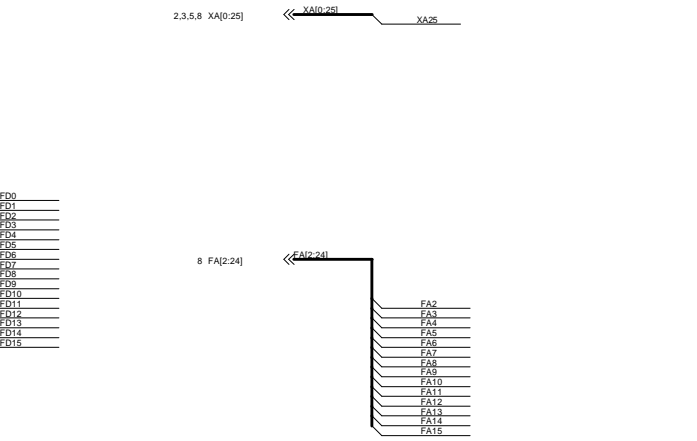
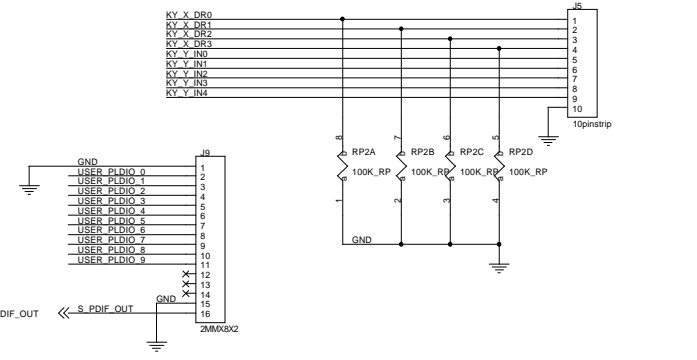
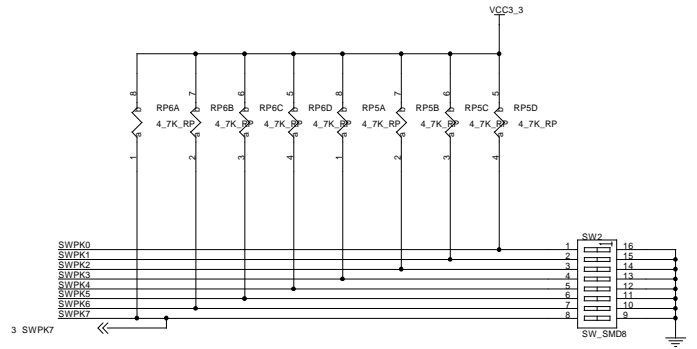
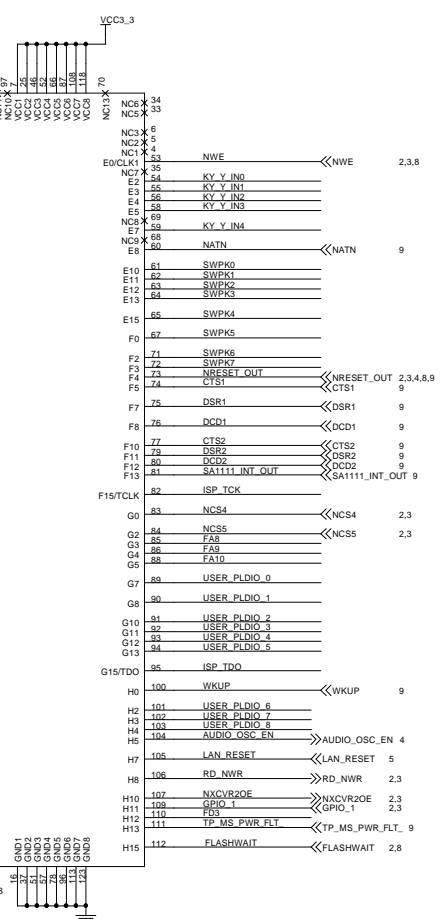
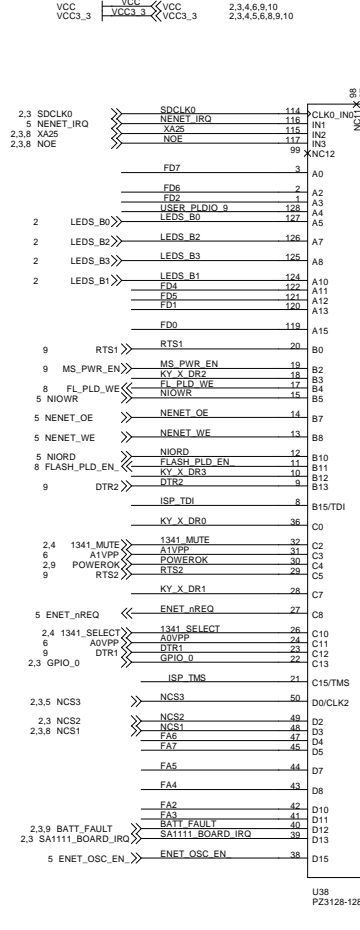
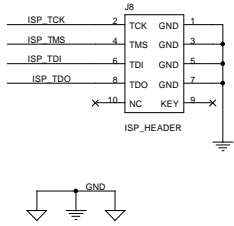
USB		SA1111 PCMCIA INTERFACE	
S1_PREG	H16	S1_PREG	S0_NPREG
S1_A0	H14	S1_A0	A11
S1_A1	H13	S1_A1	S0_PREG
S1_A2	H12	S0_A0	D11
S1_A3	H11	S0_A1	S0_A0
S1_A4	G14	S0_A2	B11
S1_A5	G12	S0_A3	S0_A1
S1_A6	G16	S0_A4	B10
S1_A7	F12	S0_A5	S0_A3
S1_A8	F14	S0_A6	C9
S1_A9	F16	S0_A7	E9
S1_A10	D14	S0_A8	S0_A4
		S0_A9	B9
		S0_A10	S0_A5
		S0_A11	C8
		S0_A12	E8
		S0_A13	S0_A6
		S0_A14	B8
		S0_A15	S0_A7
		S0_A16	A9
		S0_A17	S0_A8
		S0_A18	S0_A9
		S0_A19	S0_A10
		S0_A20	S0_A11
		S0_A21	S0_A12
		S0_A22	S0_A13
		S0_A23	S0_A14
		S0_A24	S0_A15
		S0_A25	S0_A16
S1_DATA0	J12	S1_DATA0	A12
S1_DATA1	K12	S1_DATA1	S0_DATA0
S1_DATA2	L13	S1_DATA2	C12
S1_DATA3	D13	S1_DATA3	S0_DATA1
S1_DATA4	B13	S1_DATA4	E11
S1_DATA5	A14	S1_DATA5	C11
S1_DATA6	B14	S1_DATA6	S0_DATA2
S1_DATA7	B16	S1_DATA7	E10
S1_DATA8	K13	S1_DATA8	C10
S1_DATA9	K16	S1_DATA9	S0_DATA3
S1_DATA10	E14	S1_DATA10	E09
S1_DATA11	C13	S1_DATA11	D10
S1_DATA12	E13	S1_DATA12	S0_DATA4
S1_DATA13	A15	S1_DATA13	D09
S1_DATA14	B15	S1_DATA14	S0_DATA5
S1_DATA15	C14	S1_DATA15	E08
S1_NCD1	L12	S1_NCD1	E2
S1_NCD2	L16	S1_NCD2	G5
S1_RDY	F13	S1_RDY	F8
S1_NCE1	C15	S1_NCE1	B2
S1_NCE2	C16	S1_NCE2	C3
S1_NOE	D15	S1_NOE	S0_NCE1
S1_NWE	F16	S1_NWE	S0_NCE2
S1_NIORD	D16	S1_NIORD	S0_NWE
S1_NIOWR	H14	S1_NIOWR	C9
S1_NWAIT	H14	S1_NWAIT	D4
S1_NIOIS16	G15	S1_NIOIS16	D10
S1_RESET	G13	S1_RESET	D11
S1_BVD1	J12	S1_BVD1	A13
S1_BVD2	J16	S1_BVD2	A10
S1_NV_S1	K14	S1_NV_S1	E10
S1_NV_S2	K15	S1_NV_S2	E4
			E3
GPIO_A0	H5	GPIO_A0	
GPIO_A1	F3	GPIO_A1	
GPIO_A2	F4	GPIO_A2	
GPIO_A3	F1	GPIO_A3	

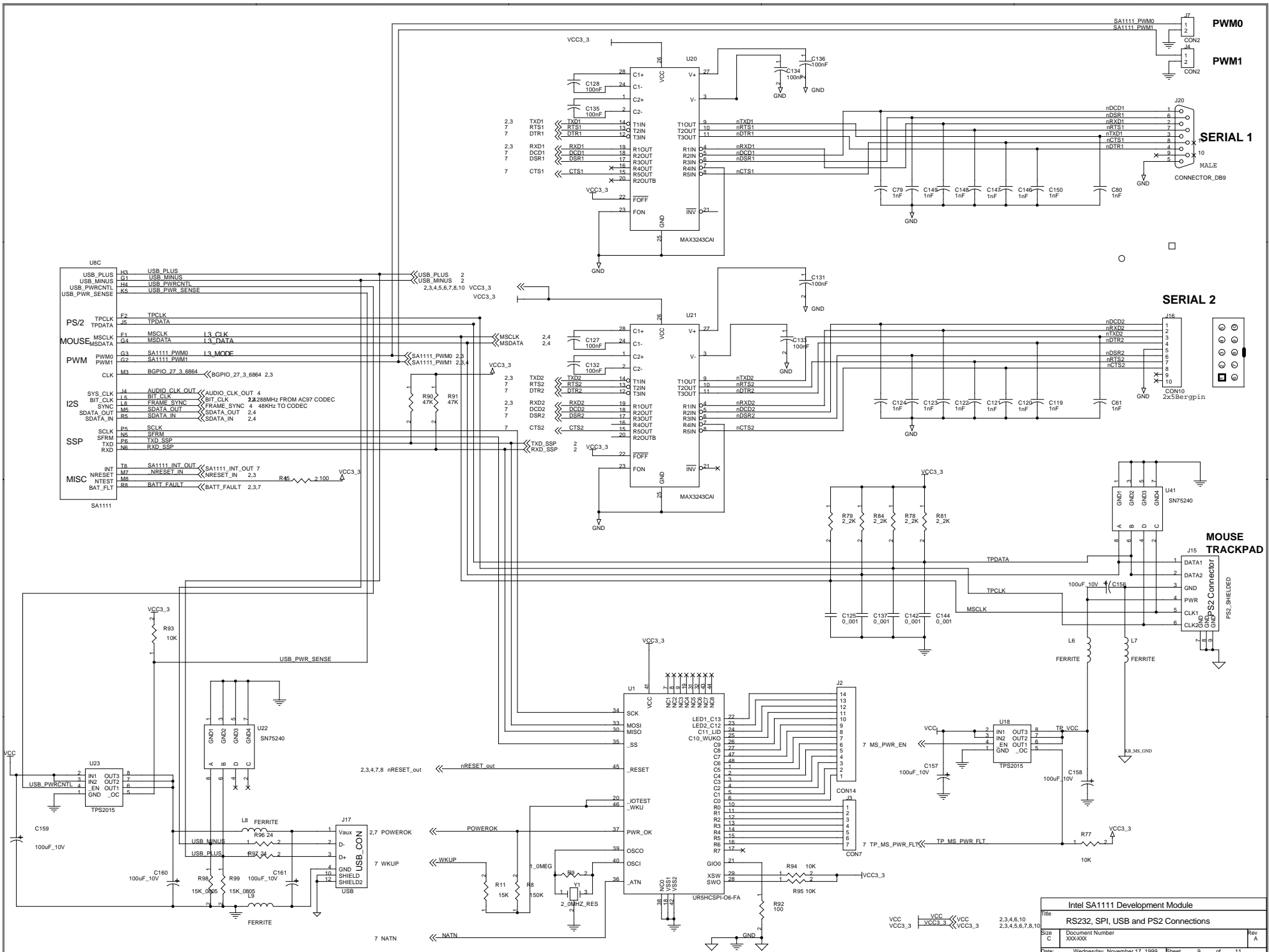


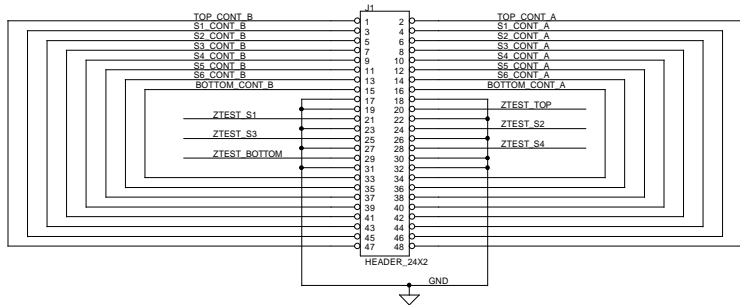
OUTER SLOT



INNER SLOT
COMPACT FLASH







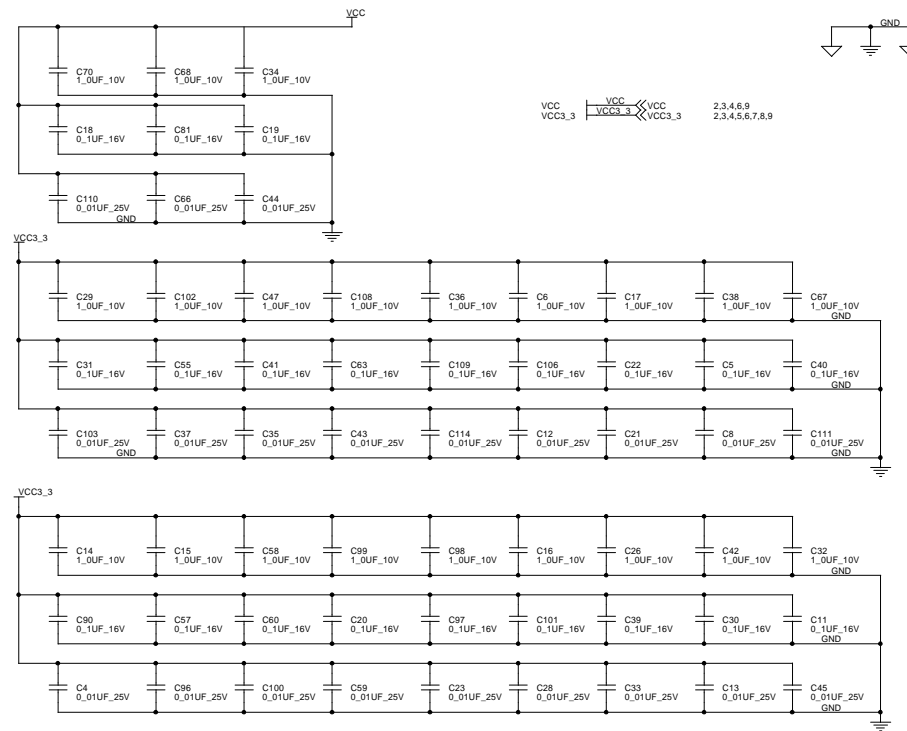
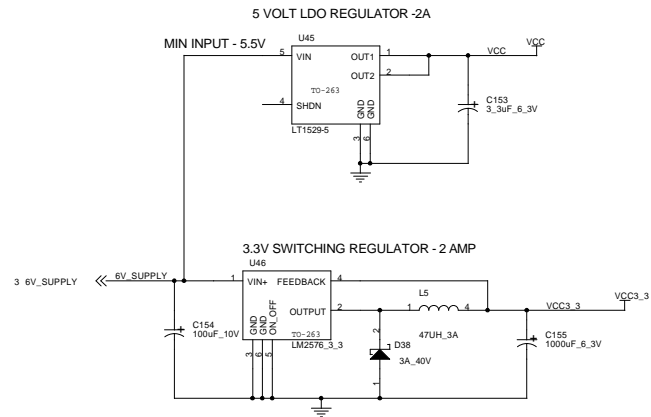
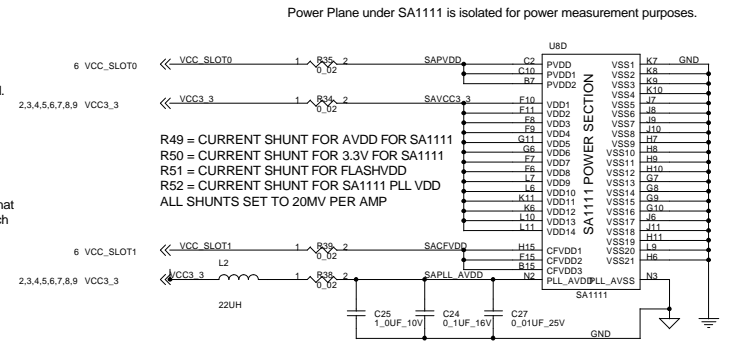
NO STUFF

Board test coupon

TEST HEADER IS 25 MIL PAD WITH 10 MIL DRILL SPACED 50 MIL SEPERATION. PATTERN IS 20 X 2 PLACED NEAR BOARD EDGE

ZTEST_layer line set to nominal line widths on each layer - minimum length = 6 Inches. These traces should be surrounded by theiving traces space 40 mils from test trace where possible. Nominal impedance should be 60 ohms +/- 10%.

"LAYER_CONT_A" and "LAYER"_CONT_B Traces are minimum trace width, 5 mil internal, 5 mil top and bottom, and minimum seperation, 5 mil external and internal, that are run around the edge of the board on as long a path as possible. This is an overetch and underetch test.



Intel SA1111 Development Module			
POWER Supplies, Test Coupon, and MISC			
File	Document Number	Rev	A
Size	XXXXXX		
Date	Wednesday, November 17, 1999	Sheet	10 of 11