



3 VOLT FlashFile™ MEMORY

28F004S3, 28F008S3, 28F016S3

SPECIFICATION UPDATE

Release Date: February, 1999

Order Number: 297799-009

The 28F004S3, 28F008S3, and 28F016S3 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The 28F004S3, 28F008S3 and 28F016S3 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available upon request.

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Intel Corporation
P.O. Box 5937
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CG-041493

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REVISION HISTORY

Date of Revision	Version	Description
09/10/96	-001	Document includes all known errata to date (original version)
12/01/96	-002	Removed CE# glitch sensitivity erratum Modified CE#-high erratum Added RP# Control erratum
02/01/97	-003	Removed CE#-high erratum
04/04/97	-004	Modified block locking and unlocking erratum Added PSOP pinout correction Change specification update title Added 16-Mbit I _{CCR} erratum Added 12V V _{PP} time specification change
05/06/97	-005	Removed 12V V _{PP} time specification change
06/05/97	-006	Added 16-Mbit block locking and unlocking erratum
08/02/97	-007	Changed status of Erratum #1, Deep Power-Down Current Changed status of Erratum #2, Block Locking and Un-Locking Changed status of Erratum #5, RP# Control during Power-Up
09/10/97	-008	Added specification clarification, "V _{PP} Program and Erase Voltages on Sub 0.4μ S3 Memory Family"
02/16/99	-007	Previous Documentation Change indicating PSOP pinout graphic error deleted; incorporated into <i>3 Volt FlashFile™ Memory</i> ; 28F004S3, 28F008S3, 28F016S3 datasheet. Specification Update renamed from <i>Byte-Wide Smart 3 FlashFile™ Memory Family Specification Update</i> . Reference to datasheet modified to reflect new datasheet name.



PREFACE

The Intel® Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published. Functional descriptions for this product are found in the *3 Volt FlashFile™ Memory; 28F004S3, 28F008S3, 28F016S3* datasheet.

Affected Documents/Related Documents

Title	Order
<i>3 Volt FlashFile™ Memory; 28F004S3, 28F008S3, 28F016S3</i> datasheet	290598-005

Nomenclature

Errata are design defects or errors. These may cause the behavior of these products to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to *3 Volt FlashFile™ Memory; 28F004S3, 28F008S3, 28F016S3* datasheet. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.
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Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.
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Errata

#	Density						Page	Status	Errata
	4-Mbit Steppings	8-Mbit Steppings				16-Mbit Steppings			
	A-0	A-1, A-3	A-6	A-8	B-0	A-0			
1		X	X	X			7	Fixed	Deep Power-Down Current
2		X	X	X			8	Fixed	Block Locking and Unlocking
3		X	X				9	Fixed	CE#-High Time
4		X					10	Fixed	CE# Glitch Sensitivity
5		X	X	X			12	Fixed	RP# Control during Power-Up
6						X	13	Eval	Active Read Current

Specification Changes

#	Density						Page	Status	Specification Changes
	4-Mbit Steppings	8-Mbit Steppings				16-Mbit Steppings			
	A-0	A-1, A-3	A-6	A-8	B-0	A-0			
N/A							14		None in this Specification Update revision.

Specification Clarifications

#	Density						Page	Status	Specification Clarifications
	4-Mbit Steppings	8-Mbit Steppings				16-Mbit Steppings			
	A-0	A-1, A-3	A-6	A-8	B-0	A-0			
1	X	X	X	X	X	X	14	Doc	V _{PP} Program and Erase Voltages on Sub 0.4μ 3 Volt FlashFile™ Memory

Documentation Changes

#	Document Revision	Page	Status	Documentation Changes
N/A				None in this Specification Update revision.



IDENTIFICATION INFORMATION

Markings

The Finished Processing Order (FPO) number correlates to a specific device stepping as illustrated in the table below:

Density	Stepping ^(1,2)	Identifier
4-Mbit	A-0	Ninth digit on topside FPO mark (third line) = Any alphabetic letter
8-Mbit	A-1,-3	Ninth digit on topside FPO mark (third line) = J, K, L, M, or N
	A-6	Ninth digit on topside FPO mark (third line) = P or Q
	A-8	Ninth digit on topside FPO mark (third line) = U or V
	B-0	Ninth digit on topside FPO mark (third line) = W
16-Mbit	A-0	Ninth digit on topside FPO mark (third line) = Any alphabetic letter

NOTE:

1. Device steppings are based on continuous updates made in manufacturing and testing of the device and represent the current material shipped.
2. 8-Mbit A-0, -2, -4, -5, and -7 material was never sampled.

ERRATA

1. Deep Power-Down Current

PROBLEM: I_{CCD} deviates from the published specification. Please replace the existing datasheet specification with the following information:

Sym	Parameter	Notes	2.7 V V_{CC}		3.3 V V_{CC}		Unit	Test Conditions
			Typ	Max	Typ	Max		
I_{CCD}	V_{CC} Deep Power-Down Current	1		12		12	μA	RP# = GND \pm 0.2 V I_{OUT} (RY/BY#) = 0 mA

NOTES:

- All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).

IMPLICATION: The increased current requirements may have an impact on power supply loading or battery life.

WORKAROUND: None.

STATUS: This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected stepping(s).

AFFECTED PRODUCTS: Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

2. **Block Locking and Unlocking**

PROBLEM: For the 8- and 16-Mbit devices that are effected by this erratum, the block unlocking security feature is currently nonfunctional. Attempts to unlock blocks, using the clear block lock-bits command sequence, may cause subsequent program and/or block erase failures. The failure is seen as a device protection error in the status register.

IMPLICATION: Block unlocking feature is disabled. This erratum effects the following command, Clear Block Lock-Bits. Locking blocks using the Set Block Lock-bits command (while RP# is equal to 12 volts) is still supported.

WORKAROUND: To prevent accidental software block lock-bit clearing, Intel permanently sets the master lock-bit during the test flow. This disables the ability to lock and unlock blocks via software only with RP# = V_{IH} . Block locking and unlocking requires 12 V on the component's RP# input when the master lock-bit is set. Don't execute the clear block lock-bits command sequence when 12 V is applied to RP#. Instead, simply override the block locking mechanism by applying 12 V to RP# to enable program/erase operations that target locked blocks.

If data security is of utmost importance, lower V_{PP} voltage equal to or less than V_{PPLK} during normal operations. With V_{PP} equal to or less V_{PPLK} , the device is protected against all data manipulation operations.

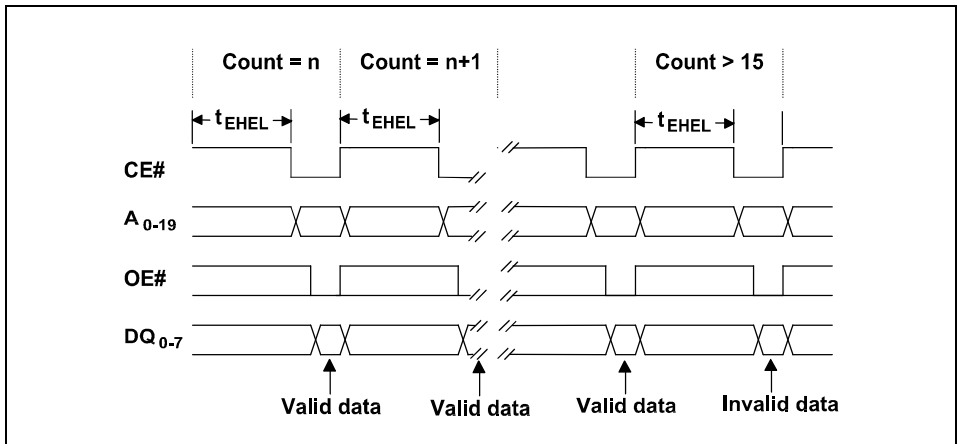
STATUS: This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected stepping(s).

AFFECTED PRODUCTS: 8-Mbit A-1, -3, -6, and -8 steppings and 16-Mbit A-0 stepping produced before work week 22 of 1997 (second digit on topside FPO marking specifies the last digit in the year and the third and fourth indicate the work week) are affected by this erratum.

3. CE#-High Time

PROBLEM: The component may return invalid data if more than fifteen successive read operations are performed where CE# is deasserted between each read and the corresponding CE#-high pulse width resides within the specifications outlined in the table below.

Stepping	CE#-High Pulse Width ($t_{EH\text{EL}}$)	
	Min	Max
A-1 and -3	100 ns	40 μs
A-6	240 ns	700 ns



Successive Read Operations That Have Long CE#-High Pulse Widths

Read the implications section, which follows, to determine whether or not your design may be affected by this erratum.

IMPLICATION: If it is determined that CE#-high time violations occur, carefully examine subsequent reads. If the ratio of good to bad (CE#-high times within the specifications outlined in the table above) reads is high, your system may not have a problem. For every bad read the system performs, five good reads for A-1 and A-3 stepping and two good reads for A-6 stepping are needed to cancel the effect of the bad read. So, carefully analyze the flash memory CE# input to understand the CE#-high characteristic.

WORKAROUND: If it is determined that your system can produce this CE#-high occurrence, here are solutions to help work around this erratum:

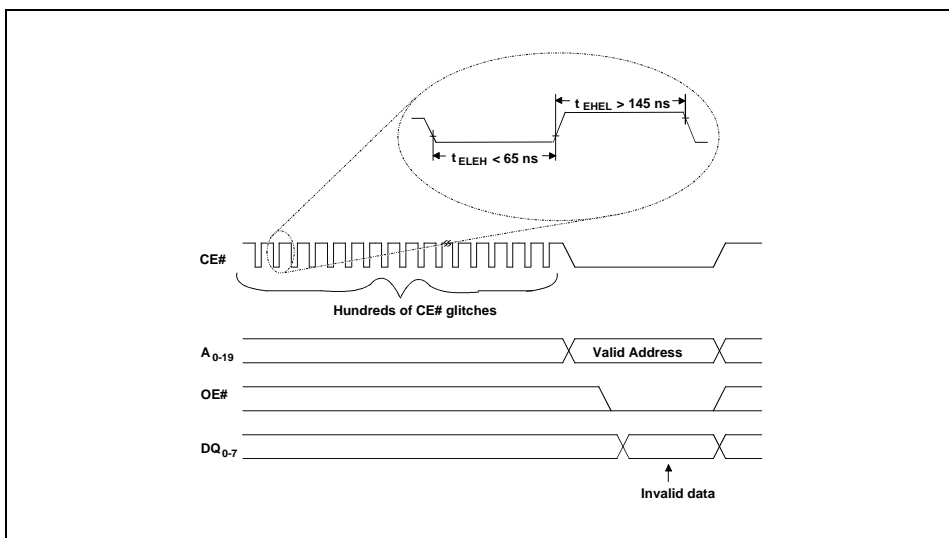
1. Read more than four good reads for A-1 and A-3 stepping and only one read for A-6 stepping during each assertion of CE#, as illustrated in the figure above.
2. Issue a Byte Write command and program FFh to any location before executing a read operation. Programming FFh will not alter stored data, but it will give the component sufficient time to prepare for the read operation.

STATUS: This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected stepping(s).

AFFECTED PRODUCTS: Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

4. CE# Glitch Sensitivity

PROBLEM: A noisy CE# control signal may cause an invalid read. This erroneous read only occurs after the device has received over one hundred consecutive short CE# glitches ($t_{EHL} < 65$ ns) with CE#-high time (t_{EHL}) greater than 145 ns (see the figure below, *A Long Series of CE# Glitches May Induce an Invalid Read*).



A Long Series of CE# Glitches May Induce an Invalid Read

After valid data is read, the device must receive another series of CE# glitches (typically over one hundred) to induce an invalid read.

IMPLICATION: This erratum may affect read operations in systems that have a lot of noise on the flash memory's CE# input. If CE# is generated asynchronously from the upper address lines, noise on CE# can sometimes occur when upper address lines transition from one state to another. However, applications that access flash memory sequentially will have stable upper address lines and will therefore produce fewer CE# glitches. Systems that execute code from flash memory or download code from flash memory into DRAM will usually access the device sequentially; therefore, they will be less susceptible to this erratum.

Carefully analyze the flash memory CE# input. If glitches are detected, more in-depth system characterization is needed to identify susceptibility to this erratum.

It is important to understand how these glitches manifest themselves in order to determine whether or not they will cause a problem.

1. In systems that flow unlatched addresses to CE# control logic, the decode logic may generate CE# glitches when the address bus transitions from one state to another. However, the processor's address switching frequency is usually very fast (somewhere in the order of 1/2 the processor's operating frequency) which will cause the glitch high time to be less than 145 ns. If the CE#-high time is less than 145 ns, the glitch has no effect on the component.

Note: Most processor's with integrated chip select logic use latched outputs and therefore may not have CE# glitches.

2. If the address bus is not pulled up or pulled down during idle bus cycles, the address bus may be left in an undetermined state. This condition may cause CE# glitches.

WORKAROUND: If it is determined that the CE# causes a problem, possible solutions to help workaround this erratum are suggested as follows.

Hardware solution:

Add system logic to prevent CE# glitches such as latched CE# control logic or pullup/pulldown resistors to the address bus.

Software solution for data storage applications:

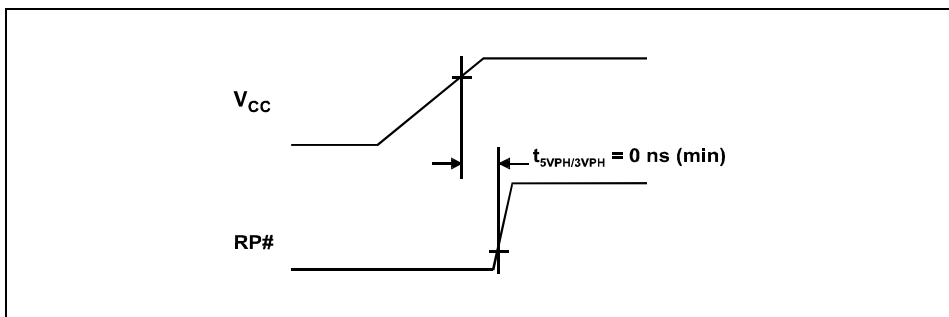
If the device receives over one hundred consecutive CE# glitches, issue a Byte Write command and program FFh to any location before executing a read operation. Programming FFh will not alter stored data, but it will give the component sufficient time to prepare for the read operation.

STATUS: This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected stepping(s).

AFFECTED PRODUCTS: Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

5. **RP# Control during Power-Up**

PROBLEM: RP# must be held low while V_{CC} ramps to a valid level during power transitions.



Hold RP# Active While V_{CC} Ramps

Holding RP# low during power-up blocks spurious writes initiated by system control logic which may occur as the system voltage transitions to a stable level. Intel recommends the use of RP# for CPU/memory reset synchronization, write protection, and deep power-down mode.

IMPLICATION: This erratum only affects power-up operations. Systems that tie the flash memory's RP# input to the system RESET# signal typically will not have a problem with erratum because the RESET# signal is usually held low during the power-up sequence to properly synchronize the CPU. However, systems that tie RP# directly to V_{CC} will be more exposed to this problem. So, carefully analyze RP# during the power-up condition to fully understand its behavior.

WORKAROUND: If it is determined that this erratum may cause a problem, here is a possible workaround:

Use a simple RC delay network to hold RP# low during the power-up condition or tie the RP# input to the system RESET# signal. This workaround will eliminate your exposure to this problem and also provide your design with addition power-up security.

STATUS: This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected stepping(s).

AFFECTED PRODUCTS: Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

6. Active Read Current

PROBLEM: I_{CCR} deviates from the published specification. Please replace the existing datasheet specification with the following information:

Sym	Parameter	Notes	2.7 V V_{CC}		3.3 V V_{CC}		Unit	Test Conditions
			Typ	Max	Typ	Max		
I_{CCR}	V_{CC} Read Current	1,2,3		15		15	mA	CMOS Inputs $V_{CC} = V_{CC} \text{ Max}$, CE# = GND $f = 5 \text{ MHz}$, $I_{OUT} = 0 \text{ mA}$

NOTES:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).
2. Automatic Power Savings (APS) reduces typical I_{CCR} to 3 mA in static operation.
3. CMOS inputs are either $V_{CC} \pm 0.2V$ or $GND \pm 0.2V$. TTL inputs are either V_{IL} or V_{IH} .

IMPLICATION: The increased current requirements may have an impact on power supply loading or battery life.

WORKAROUND: None.

STATUS: Plans to fix this erratum are under evaluation Refer to the *Summary Tables of Changes* to determine the affected stepping(s).

AFFECTED PRODUCTS: Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

SPECIFICATION CHANGES

There are no specification changes in this Specification Update revision.

SPECIFICATION CLARIFICATIONS

1. *V_{PP} Program and Erase Voltages on Sub-0.4 μ 3 Volt FlashFile™ Memory Family*

The Intel® 3 Volt FlashFile memory (x8) family provides in-system program/erase at 3.3 V V_{PP} and faster factory program/erase at 12 V V_{PP}.

Future sub-0.4 μ lithography 3 Volt FlashFile memory products will also include a backward-compatible 12 V programming feature. This mode, however, is not intended for extended use. A 12 V program/erase V_{PP} can be applied for 1000 cycles maximum per block or 80 hours maximum per device. To ensure compatibility with future sub-0.4 μ 3 Volt FlashFile memory products, present designs should not permanently connect V_{PP} to 12 V. This will avoid device over-stressing that may cause permanent damage.

DOCUMENTATION CHANGES

There are no documentation changes in this Specification Update revision.