

Infrared Data Association

RECOMMENDED SERIAL INTERFACE FOR TRANSCEIVER CONTROL



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Author:

Franco Iacobelli (National Semiconductor Corporation)

Significant Contributors:

John Petrilla, Takashi Hidai (Agilent Technologies Inc.)

Bryn Owen, Patrick Kam (IBM Corporation)

Ray Chock (Calibre Inc.)

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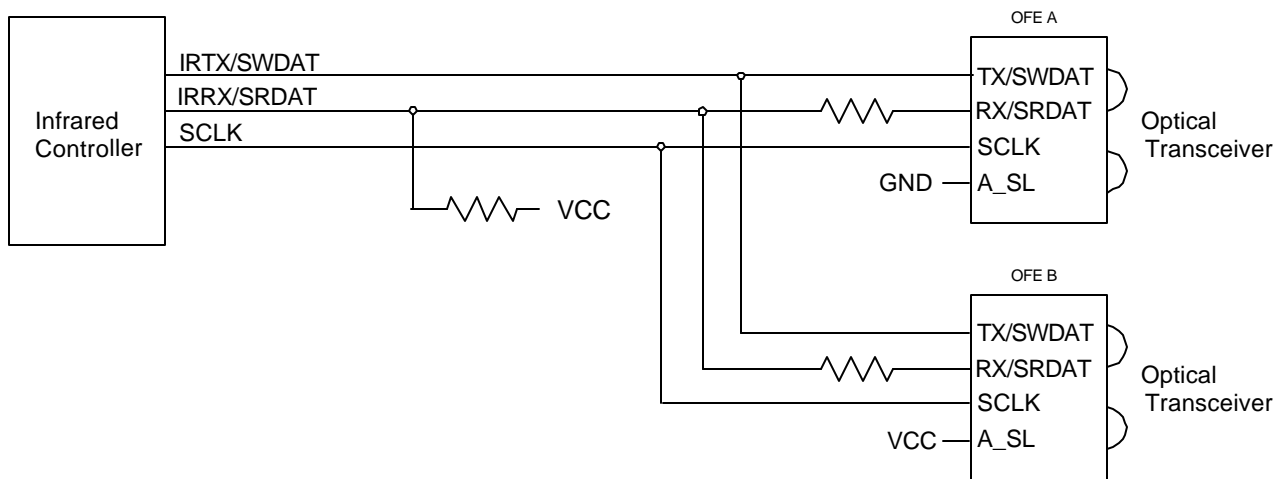
1.1 OVERVIEW

This document describes a simple serial interface that allows an infrared controller to communicate with one or more infrared transceivers. This interface requires three signals: a clock line that is used for timing, and two unidirectional lines multiplexed with the transmitter (write) and receiver (read) infrared signal lines. The main features of the serial interface are listed below.

- Message Based
- Low Power Consumption
- High Speed
- Simple Protocol
- Bus protocol implemented in hardware or in software through bit banging.
- Read and write capability
- Open Architecture (not patented)
- Easily Expandable

1.2 BASIC CONFIGURATIONS

There are two basic system configurations using the serial interface. The first one is found in portable computers and most embedded systems. In this case two optical transceivers are typically used; one in the front and one in the rear of the system's chassis. Furthermore, the infrared controller and transceivers are in close proximity of one another. The interconnections are usually implemented with single ended signals since their contribution to EMI is minimal. Handling multiple optical transceivers is easily accomplished by assigning them different addresses. The second configuration exists typically in desktop systems. In this case only one transceiver is required. The transceiver is usually mounted on a tiny PC board and communicates with the infrared controller through a shielded cable approximately 1.5 m long. This PC board and cable assembly is commonly referred to as Infrared Dongle. Currently existing Dongles use single ended signaling. However, due to the inherent EMI problems of this arrangement, there is a strong incentive in future Dongles to use differential signaling.



Figures 1-1 and 1-2 below show two typical transceiver configurations.

Figure 1-1. Interface to Two Infrared Transceivers.

The data lines are multiplexed with the transmitter and receiver signals and a different address for each transceiver can be selected. The pullup resistor on the IRRX/SRDAT line is used to prevent spurious low-going transitions during the time in which both transceivers are disabled. When no infrared communication is in progress and the serial interface is

idle, the IRTX/SWDAT line is kept low and IRRX/SRDAT is kept high.

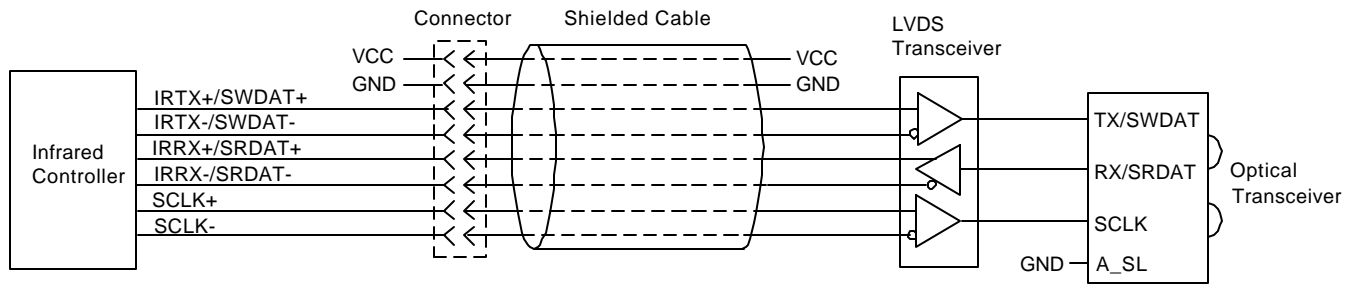


Figure 1-2. Infrared Dongle with Differential Signaling.

1.3 FUNCTIONAL DESCRIPTION

The serial interface is designed to interconnect two or more devices. One of the devices is always in control of the serial interface and is responsible for starting every transaction. This device functions as the bus master and is always the infrared controller. The infrared transceivers act as bus slaves and only respond to transactions initiated by the master. A bus transaction is made up of one or two phases. The first phase is the Command Phase and is present in every transaction. The second phase is the Response Phase and is present only in those transactions in which data must be returned from the slave. If the operation involves a data transfer from the slave, there will be a Response Phase following the Command Phase in which the slave will output the data.

The start bit of the slave response, if present, must occur 4 clock cycles after the last bit of the Command Phase, as shown in figures 1-8 and 1-9, otherwise it is assumed that there will be no response. The master must always complete the transaction normally. More precisely, it must not stop the clock and terminate the transaction earlier if the slave does not respond.

The SCLK line is always driven by the master and is used to clock the data being written to or read from the slave. This line is driven by a totem-pole output buffer. The **SCLK line is always stopped** when the serial interface is idle to minimize power consumption and to avoid any interference with the analog circuitry inside the slave. There are no gaps between the bytes in either the Command or Response Phase. Each byte of data in both Command and Response Phases is preceded by one start bit. Data is always transferred in **Little Endian** order (least significant bit first). Input data is sampled on the rising edge of SCLK. Output data from the controller is clocked by SCLK falling edge. Output data from the slave is clocked by SCLK rising edge. This makes the interface signaling less sensitive to timing skews. Figure 1-3 shows the interface timing including the data sampling points.

The data to be written to the slave is carried on the IRTX/SWDAT line. When the control interface is idle, this line carries the infrared data signal used to drive the transmitter LED. When the first low-to-high transition on SCLK is detected at the beginning of the command sequence, the slave will disable the transmitter LED. The infrared controller then outputs the command string on the IRTX/SWDAT line. On the last SCLK cycle of the command sequence the slave re-enables the transmitter LED and normal infrared transmission can resume. No transition on SCLK must occur until the next command sequence, otherwise the slave will disable the transmitter LED again.

Read data is carried on the IRRX/SRDAT line. The slave disables the internal signal from the receiver photo diode during the response phase of a read transaction. The addressed slave will output the read data on the IRRX/SRDAT line regardless of the setting of the Receiver Output Enable bit in the Mode Selection register 0. Non addressed slaves will tri-state the IRRX/SRDAT line. When the transceiver is powered up, the IRTX/SWDAT line should be kept low and SCLK should be cycled at least 30 times by the infrared controller before the first command is issued on the IRTX/SWDAT line. This guarantees that the transceiver interface circuitry will properly initialize and be ready to receive commands from the controller (note 1). In case of a multiple transceiver configuration, only one transceiver should have the receiver output enabled. If these transceivers are connected to the infrared controller via short traces (like in a notebook computer), a series resistor (approx. 200 ohms) should be placed on the receiver output from each transceiver to prevent large currents in case a conflict occurs due to a programming error.

Note 1: Since there is no reset line, the serial interface can be initialized by implementing a

self-resetting interface state machine in the transceiver. This machine must be guaranteed to transition to the idle state by cycling the SCLK line at least 30 times while keeping IRTX low. It is only from the idle state that the transceiver state machine can correctly accept a command from the infrared controller.

Figures 1-4 to 1-9 show the waveforms for the various serial interface operations.

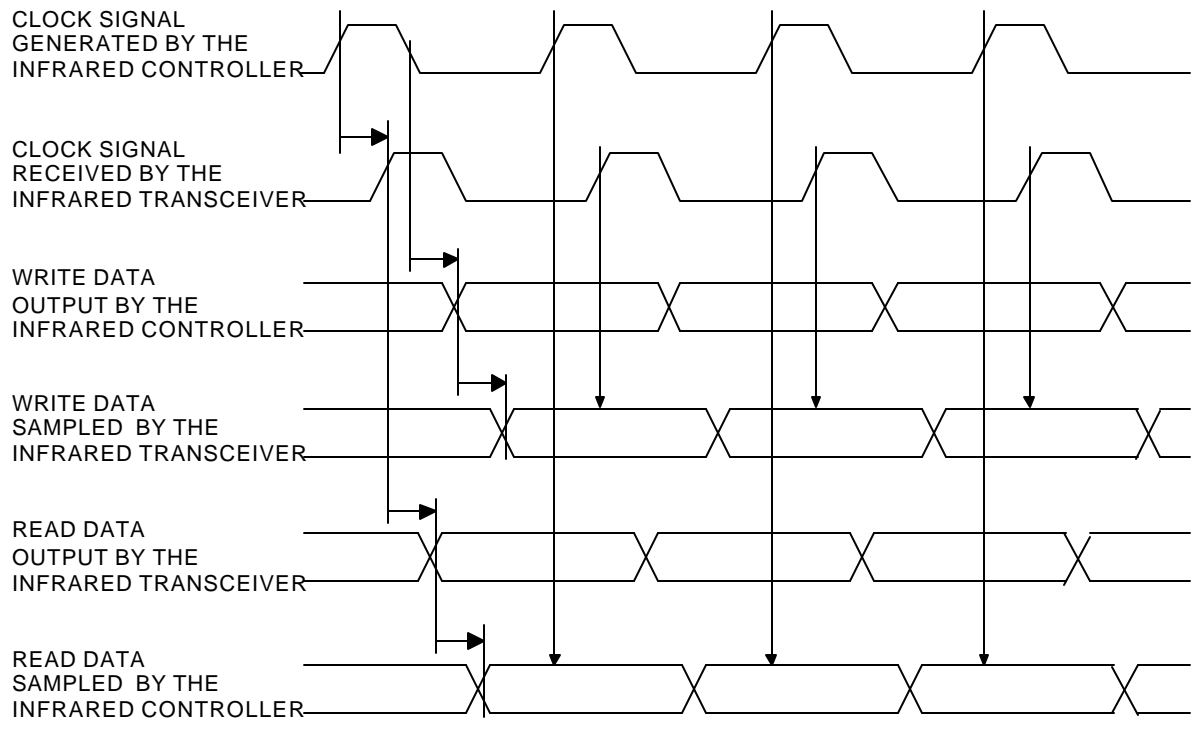


Figure 1-3. Serial Interface Timing.

This figure shows the signal delays due to the cable as well as the data sampling points for both the infrared controller and transceiver.

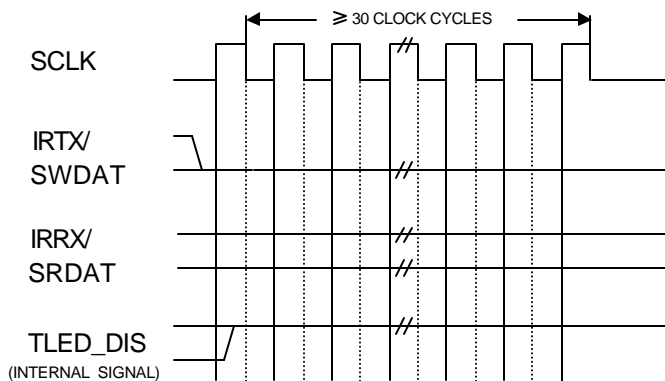


Figure 1-4. Initial Reset Timing

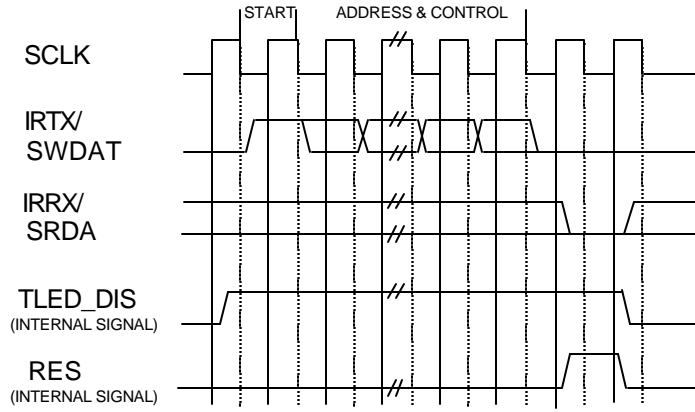


Figure 1-5. Special Command Waveform

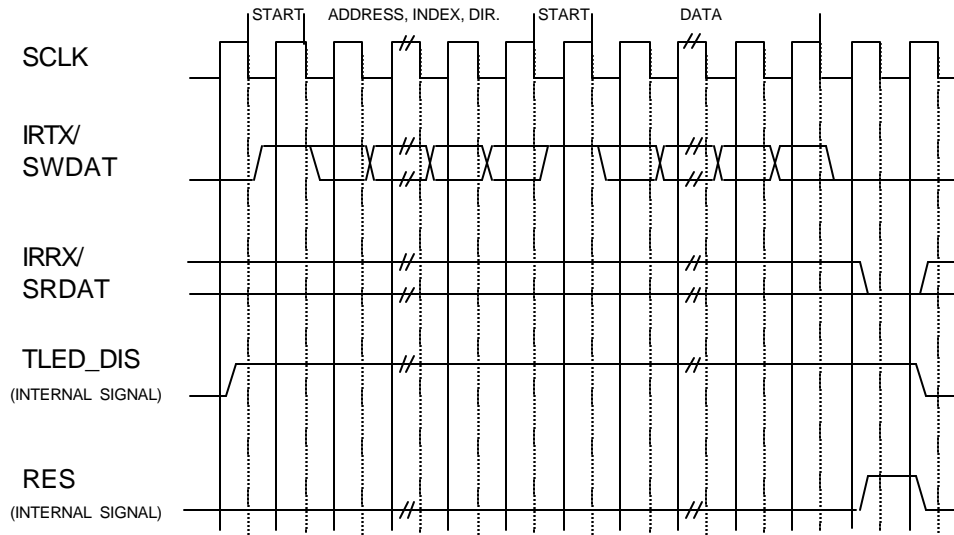


Figure 1-6. Write Data Waveform.

Note 2: If the APEN bit in control register 0 is set to 1, the internal signal from the receiver photo diode is disconnected and the IRRX/SRDAT line from the addressed transceiver is pulsed low for one clock cycle at the end of a write or special command. No pulse is generated if a broadcast address is used.

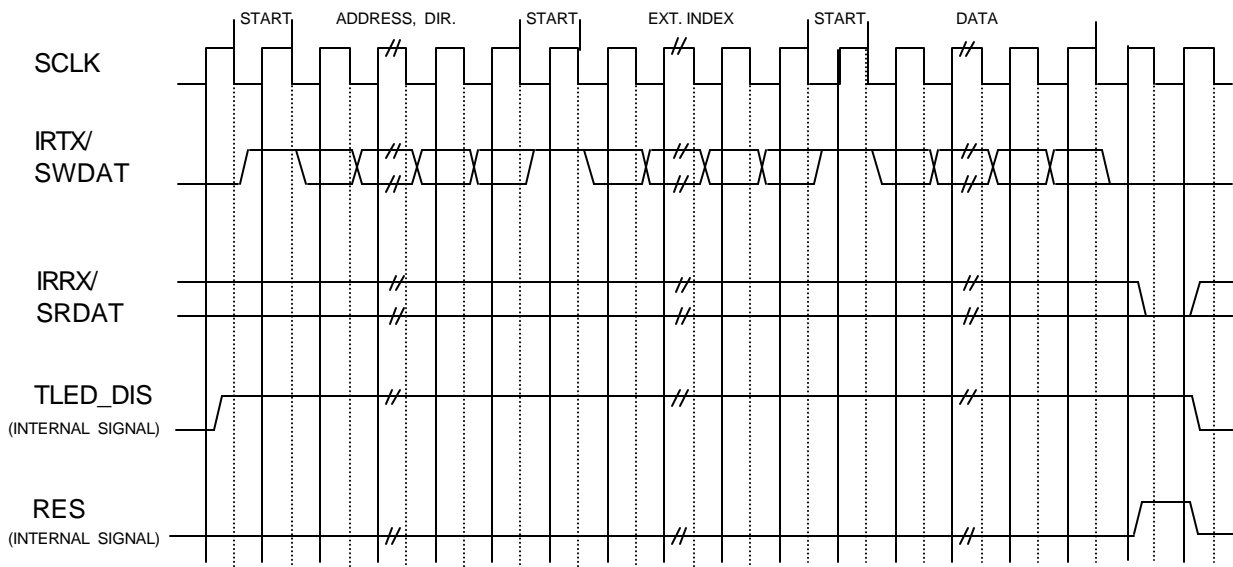


Figure 1-7. Write Data Waveform with Extended Index.

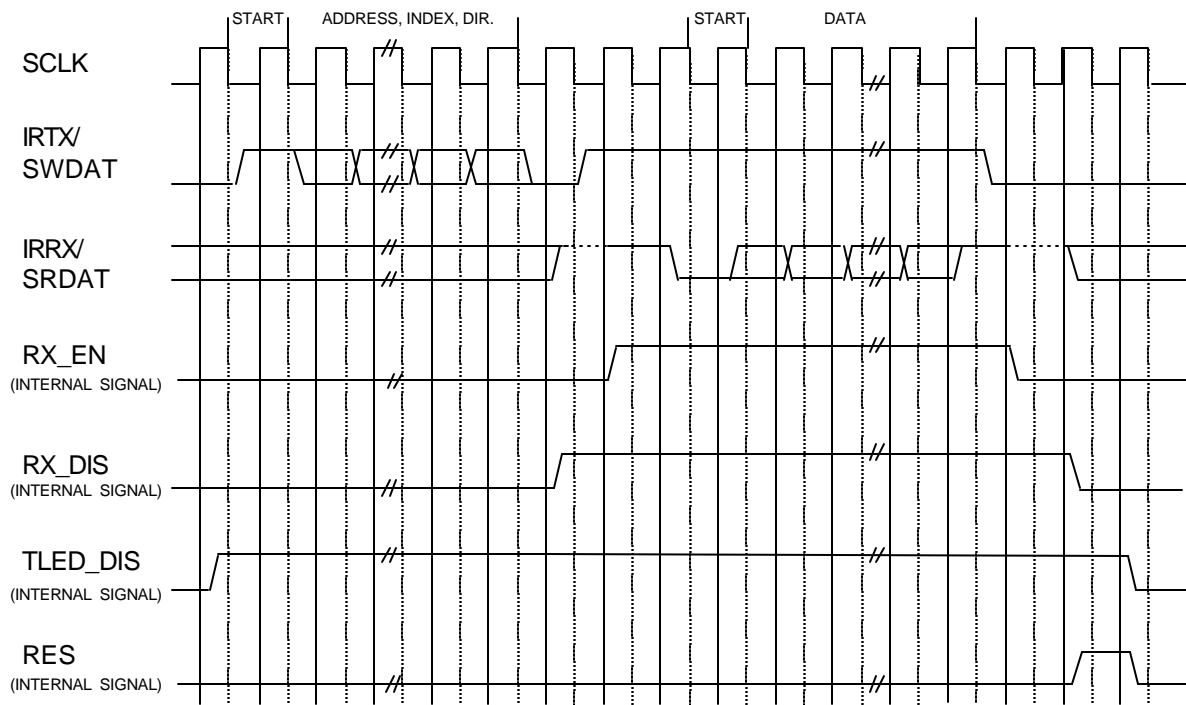


Figure 1-8. Read Data Waveform.

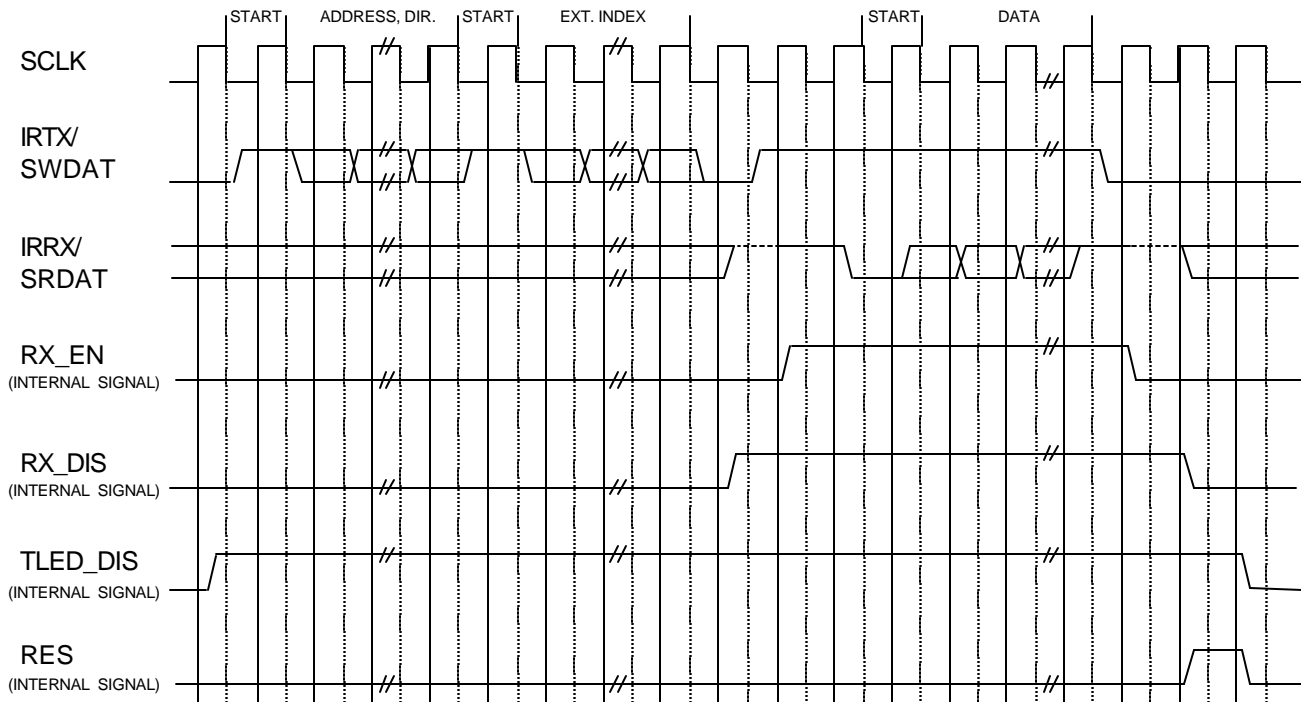


Figure 1-9. Read Data Waveform with Extended Index.

Note 3: During a read transaction the infrared controller sets the IRTX/SWDAT line low for one clock cycle after sending the address and index byte (or bytes). It will then set it high and low again three clock cycles before the end of the transaction. It is strongly recommended that optical transceivers monitor this line instead of counting clock cycles in order to detect the end of the read transaction. This will always guarantee correct operation in case two or more transceivers from different manufacturers are sharing the serial interface.

2.0 BUS PROTOCOL

A set of commands is provided to handle the various transactions between the master and each of the slaves. The set is fully expandable to handle future requirements. The general command format is shown in figure 2-1. Data is transferred in little endian order, bit 0 of byte 0 is the first bit transferred, bit 7 of byte 2 is the last.

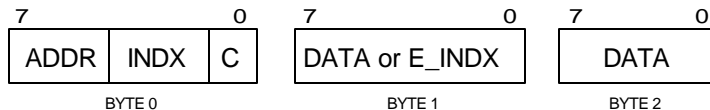


Figure 2-1. General Command Format.

The first byte, common to all transactions, contains the address of the slave to be accessed and two control fields. The first control field is the INDXX field. It determines whether the transaction is a Special Transaction or a Data Transaction. The second control field (C field) consists of only one bit and either determines the data transfer direction or it further qualifies a special transaction. The second byte is present in read and write transactions.

It contains either the data being transferred between master and slave, or the 'extended' register index. The third byte contains the data being transferred and it is only present in transactions using the extended index. A slave ignores invalid commands as well as commands specifying a register that is not implemented. Each slave responds to one or more addresses. A slave should provide one or more strap pins to select its address.

Tables 2-1 and 2-2 show the encoding for the address and INDX fields in the first command byte.

Table 2-1. Device Addressing

ADDR[2-0]	Description
000 to 101	6 Assignable Transceiver Addresses.
110	Reserved
111 (Note 1)	Broadcast Address

Note 1: A broadcast address cannot be specified for a read transaction.
A slave must ignore any read transaction with a broadcast address.

Table 2-2. Index Field and C Bit Encodings

INDX[3-0]	C Bit	Description
0000 to 1011	x (Note 2)	12 Assignable Register Indexes
1100 to 1101	0	Reserved for Additional Special Commands
1100	0	Vendor Specific Special Command
1100	1	Vendor Specific Special Command
1101	1	Reset Transceiver to Default State
1110	1	Reset AGC and Select Primary Receiver Sensitivity
1111	x (Note 2)	Escape Code for Extended Indexing

Note 2: The C bit value determines the transfer direction in all register access transactions.
C = 1: write transaction. C = 0: read transaction.

Special Transactions

Special transactions are only one byte long and are designed to control various non-data-transfer functions in the slave. Only two special transactions are currently defined. The first one is used to reset the slave's internal registers to their default state. The second one is used to reset the AGC and to select the primary receiver sensitivity at the end of a transmitted or received frame. Their formats are shown below.

Reset Slave's Internal Registers to Default State

ADDR[2:0]	1	1	0	1	1
-----------	---	---	---	---	---

Reset AGC and Select Primary Receiver Sensitivity

ADDR[2:0]	1	1	1	0	1
-----------	---	---	---	---	---

Write Data Transactions

These transactions are always required and are used to write data into the slave to select the slave's operational mode. Only the command phase is needed.

Command formats

ADDR[2:0]	INDX[3:0]	1	DATA
-----------	-----------	---	------

ADDR[2:0]	1	1	1	1	1	E_INDX[7:0]	DATA
-----------	---	---	---	---	---	-------------	------

- The ADDR field represents the slave address.
- The INDX and E_INDX fields indicate the slave's register to be written into.
- The DATA field contains the data to be written into the slave to select the operational mode.

Note: At least two distinct addresses should be supported since some notebooks use two transceivers, one in the front and one in back. This allows both transceivers to be directly attached to the serial bus.

Read Data Transactions

These transactions are implemented by the slaves in order to support Plug-n-Play or to report the currently selected mode. The data returned by a read transaction may include the slave's operational capabilities and other relevant information. Both command phase and response phase are always present in a read transaction.

Command phase formats

ADDR[2:0]	INDX[3:0]	0
-----------	-----------	---

ADDR[2:0]	1	1	1	1	0	E_INDX[7:0]
-----------	---	---	---	---	---	-------------

Slave Response format

DATA

- The ADDR field represents the slave address.
- The INDX and E_INDX fields indicate the slave's register whose data is to be returned during the response phase.
- The DATA field contains the returned data.

3.0 SLAVE INTERNAL REGISTERS

Following is a list of the internal registers that a transceiver may provide. These registers are divided into two groups as described below. Simple transceivers may implement only a subset of these registers. Transceivers do not need to respond to all transaction types or to transactions specifying a register that is not implemented. However, in order to properly operate in multiple transceiver configurations, each transceiver must follow all types of transactions occurring on the serial interface.

Main Control Registers

These registers belong to the first group and are addressed by a 4-bit index field. They are used to control the operational mode of the transceiver. Some bits are used to enable special features and need not be implemented by all transceivers. All the implemented registers must support write accesses. Read accesses are optional.

INDX[3-0]	Selected Register										
0	<p>Control Register 0. (read/write) Upon reset, all implemented bits are set to 0.</p> <p>bit 0 PM_SL - Power Mode Select. 0 => low power mode (sleep mode) 1 => normal operation power mode</p> <p>bit 1 RX_OEN - Receiver Output Enable 0 => IRRX/SRDAT line disabled (tri-stated) 1 => IRRX/SRDAT line enabled</p> <p>bit 2 TLED_EN - Transmitter LED Enable 0 => disabled 1 => enabled</p> <p>bit 3 DM_EN - CIR/Sharp-IR Demodulation Enable, (Optional). This bit is optional and may be implemented in transceivers supporting Consumer-IR and/or Sharp-IR modes. 0 => envelope demodulation disabled 1 => envelope demodulation enabled</p> <p>bit 4 APEN - Acknowledge Pulse Enable, (Optional). This bit is used to enable the acknowledge pulse. When it is set to 1 and RX_OEN is 1 (receiver output enabled), the IRRX/SRDAT line will be pulsed low for one clock cycle upon successful completion of every write command or special command with individual (non broadcast) transceiver address. The internal signal from the receiver photo diode is disconnected when this bit is set to 1.</p> <p>bit 5 AGCMSK - AGC Mask Enable, (Optional). When set to 1, the internal signal from the receiver diode is prevented from reaching the AGC circuitry while the transmitter signal is active. This can be used to detect infrared traffic from other sources while a frame is being transmitted.</p> <p>bit 6 reserved</p> <p>bit 7 TAUX_EN - Transmitter Auxiliary Output Enable, (Optional). This bit is used by those transceivers providing an auxiliary output signal to drive an external transmit LED. When this bit is set to 1, the auxiliary output signal is enabled.</p>										
1	<p>Control Register 1. (read/write)</p> <p>bits 7-0 Infrared Mode Selection. The value to be written into this register to select a certain infrared mode is the same as the bit offset value of the bit indicating support for that mode. The offset value is calculated from bit 0 of the register at extended index 7. Upon reset, all implemented bits are set to 0 selecting the SIR mode. Example encodings are shown below.</p> <table border="0" style="margin-left: 40px;"> <tr><td>0</td><td>SIR</td></tr> <tr><td>1</td><td>MIR</td></tr> <tr><td>2</td><td>FIR</td></tr> <tr><td>3</td><td>AppleTalk</td></tr> <tr><td>4</td><td>Air</td></tr> </table>	0	SIR	1	MIR	2	FIR	3	AppleTalk	4	Air
0	SIR										
1	MIR										
2	FIR										
3	AppleTalk										
4	Air										

5	VFIR-16
6	VFIR-TBD
7	VFIR-TBD
8	Sharp-IR
32	36 kHz CIR

Note: The following control registers are optional. A transceiver manufacturer may choose to implement only a subset of the bits in any of these registers. However, in order to guarantee software transparency, implemented bits should start from the most significant bit position.

Both Power Level and Receiver Sensitivity settings are binary encoded.

For example, if it is desired to have a total of eight power levels, then each level can be represented as a binary combination of I2, I1 and I0. This combination is then mapped into the control register, starting with the most significant bit.

Control Register 2, bit 7 <= I2

Control Register 2, bit 6 <= I1

Control Register 2, bit 5 <= I0

The least significant five bits are then left unused and return zeros when read.

2 Control Register 2. (read/write)
Upon reset, all implemented bits are set to 1 selecting the standard SIR power level.

bits 7-0 Transmitter Power Level

All 0's => Minimum output power level

All 1's => Maximum output power level

3 Control Register 3. (read/write).
This register holds the primary receiver sensitivity.
Writing into this register will select the primary sensitivity.
Upon reset, bit 7 is set to 0 and all the other implemented bits are set to 1 selecting the standard SIR sensitivity.

bits 7-0 Primary Receiver Sensitivity.

All 0's => Highest Sensitivity (lowest threshold)

All 1's => Lowest Sensitivity

4 Control Register 4. (read/write).
This register holds the alternate receiver sensitivity.
Writing into this register will select the alternate sensitivity.
Upon reset, bit 7 is set to 0 and all the other implemented bits are set to 1 selecting the standard SIR sensitivity.

bits 7-0 Alternate Receiver Sensitivity.

All 0's => Highest Sensitivity (lowest threshold)

All 1's => Lowest Sensitivity

5 - 11 These registers are currently reserved.

Extended Indexed Registers

These registers form the second group and are addressed by an 8-bit extended index. They are mainly used for transceiver identification or for vendor specific purposes.

Except for two registers, the implementation of these registers is optional. The two registers with extended index values of 0 and 1 are mandatory since they are used by the infrared software driver to identify the transceiver.

E_INDIX[7-0] Selected Register

- 0 Manufacturer's ID
This register returns a value identifying the transceiver's manufacturer. Currently assigned values are given in table 3-1 below.

Table 3-1. Manufacturer's ID Values .

Device Manufacturer	ID Value
Agilent Technologies	01h
IBM	02h
Sharp	03h
Vishay-Telefunken	04h
Texas Instruments	05h
Novalog	06h
Unitrode	07h
Infineon	08h
Calibre	09h
Reserved	0Ah - FFh

- 1 Device ID
This register returns a value identifying the transceiver. The meanings of the various bits are described below.
 - bits 5-0 Device type and/or revision level.
This field is manufacturer's specific.
 - bit 6 Read support for non-extended registers.
This bit is set to 1 if the device supports the reading of all the main control registers.
 - bit 7 Read support for extended registers.
This bit is set to 1 if the device supports the reading of all the extended indexed registers.
- 2 - 3 Reserved
- 4 Misc. Capabilities, (read-only)
 - bits 2-0 Receiver Recovery Time After Transmit.
In the IrLAP document this parameter is referred to as the Minimum Turnaround Time.

Serial Interface for Transceiver Control

000	0	ms
001	0.01	ms
010	0.05	ms
011	0.1	ms
100	0.5	ms
101	1	ms
110	5	ms
111	10	ms

bits 3 reserved

bits 6-4 Power ON Stabilization Time.

00x	reserved
010	0.5 ms
011	1 ms
100	5 ms
101	10 ms
110	50 ms
111	reserved

bits 7 reserved

5 Misc. Capabilities (read-only)

bits 2-0 Receiver Stabilization Time for SIR, MIR, FIR, etc.
(Number of additional BOFs or preamble symbols)

000	0
001	1
010	2
011	3
100	5
101	12
110	24
111	48

bit 3 reserved

bits 6-4 Serial Interface Maximum Speed.

000	100 kHz
001	500 kHz
010	1 MHz
011	4 MHz
1xx	reserved

bit 7 reserved

Note: In the following registers (with extended index values from 6 to 14) each bit indicates whether a certain capability is supported. The capability is supported if the corresponding bit is set to 1.

6 Misc. Capabilities (read-only)

bit 0	Low power mode support.
bit 1	Support for programmable transmitter power level
bit 2	Support for programmable receiver sensitivity

- bit 3 Support for programmable alternate receiver sensitivity
- bit 4 Support for programmable receiver bandwidth
- bit 5 Programmable CIR or Sharp-IR demodulation support.
- bit 6 Support for CIR traffic monitoring while an IrDA mode is selected.
- bit 7 Support for automatic wakeup ?

7 Supported Infrared Modes (read-only)

- bit 0 SIR
- bit 1 MIR
- bit 2 FIR
- bit 3 AppleTalk
- bit 4 Alr
- bit 5 VFIR-16
- bit 6 VFIR-TBD
- bit 7 VFIR-TBD

8 Supported Infrared Modes (read-only)

- bit 0 Sharp-IR
- bits 7-1 reserved

9 Supported CIR Sub-carrier Frequencies (read-only)

- bit 0 reserved
- bit 1 CIR base band, low speed (30-57 kHz SCF)
- bit 2 CIR base band, medium speed (400-500 kHz SCF)
- bit 3 CIR base band, high speed (1-2 MHz SCF)
- bits 7-4 reserved

10 Supported CIR Sub-carrier Frequencies (read-only)

- bits 0-1 reserved
- bits 2-7 30 to 35 kHz
Each bit indicates one frequency

11 Supported CIR Sub-carrier Frequencies (read-only)

- bits 0-7 36 to 43 kHz
Each bit indicates one frequency

12 Supported CIR Sub-carrier Frequencies (read-only)

- bits 0-7 44 to 51 kHz
Each bit indicates one frequency

- 13 Supported CIR Sub-carrier Frequencies (read-only)
 - bits 0-5 52 to 57 kHz
Each bit indicates one frequency
 - bits 6-7 reserved

- 14 Supported CIR Sub-carrier Frequencies (read-only)
 - bit 0 400 kHz
 - bit 1 450 kHz
 - bit 2 480 kHz
 - bits 3-7 reserved

- 15 - 239 These registers are currently reserved.

- 240 - 255 These registers are vendor specific.

4.0 ELECTRICAL SPECIFICATIONS

Timing specifications are given in table 4-1. Only the timing parameters are specified in this document. Switching thresholds and capacitive loads are not specified since they are outside the scope of this document.

The DC characteristics are provided in the document titled 'Infrared Dongle Interface' available from IrDA.

Table 4-1. Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Max.	Units
tCKp	SCLK Clock Period	R.E., SCLK to next R.E., SCLK	250 ns	∞ (note)	
tCKh	SCLK Clock High Time	R.E., SCLK to F.E. SCLK	60		ns
tCKl	SCLK Clock Low Time	F.E., SCLK to R.E. SCLK	80		ns
tDOtv	Output Data Valid (from infrared controller)	After F.E., SCLK		40	ns
tDOth	Output Data Hold (from infrared controller)	After F.E., SCLK	0		ns
tDOrv	Output Data Valid (from optical transceiver)	After R.E., SCLK		40	ns
tDORh	Output Data Valid (from optical transceiver)	After R.E., SCLK		40	ns
tDORf	Line Float Delay	After R.E., SCLK		60	ns
tDI _s	Input Data Setup	Before R.E., SCLK	10		ns
tDI _h	Input Data Hold	After R.E., SCLK	5		ns

Note: The serial interface must be fully static and must function properly as long as the SCLK clock frequency is within the specified limits. If the clock is stopped in the middle of a transaction and then restarted at

a later time, the transaction must continue from the exact point were it was stopped.
 The interface logic must not implement any timeout. However, the transmitter LED should be timeout protected to prevent any damage in case of a protocol error.

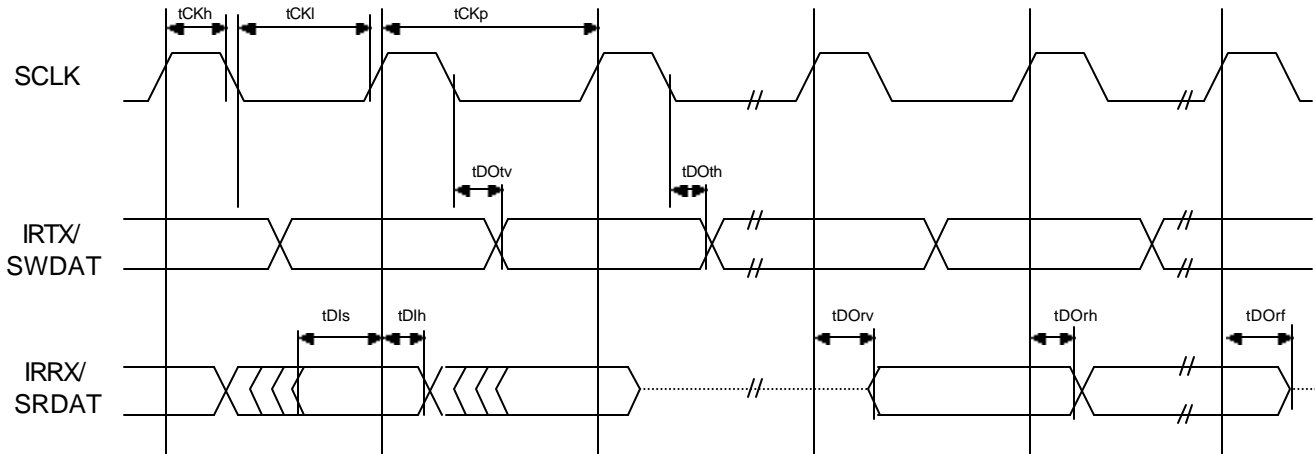


Figure 4-1. Timing Diagram

APPENDIX A

Implementation Example

Following is a simple implementation of the *slave side* serial interface. Only write transactions to the main control registers, special commands and reading of the Manufacturer's ID and Device ID registers are supported. Reading of the main control registers as well as read/write accesses to the other extended addressed registers is not supported. This implementation keeps track of read commands and commands using extended indexing so that it can coexist with future implementations.

In order to save logic, this design relies on asynchronous registers. This assumes that the signals from the state machine are glitch free. If this condition is not satisfied, then synchronous registers (e.g. with enable input) must be used instead.

Note: This implementation is not yet tested !

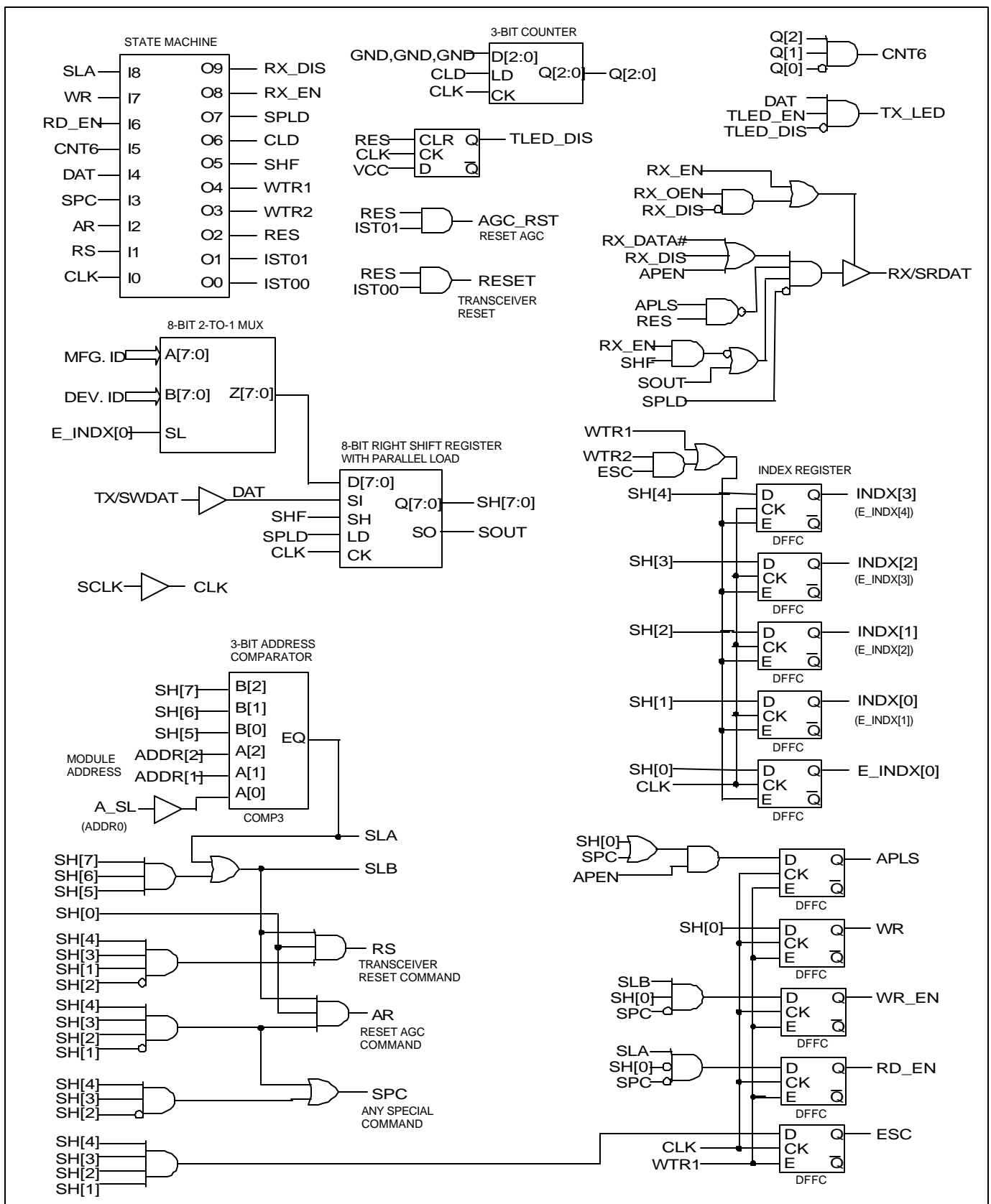


Figure A-1. Serial Interface Circuit Diagram, (Slave Side)

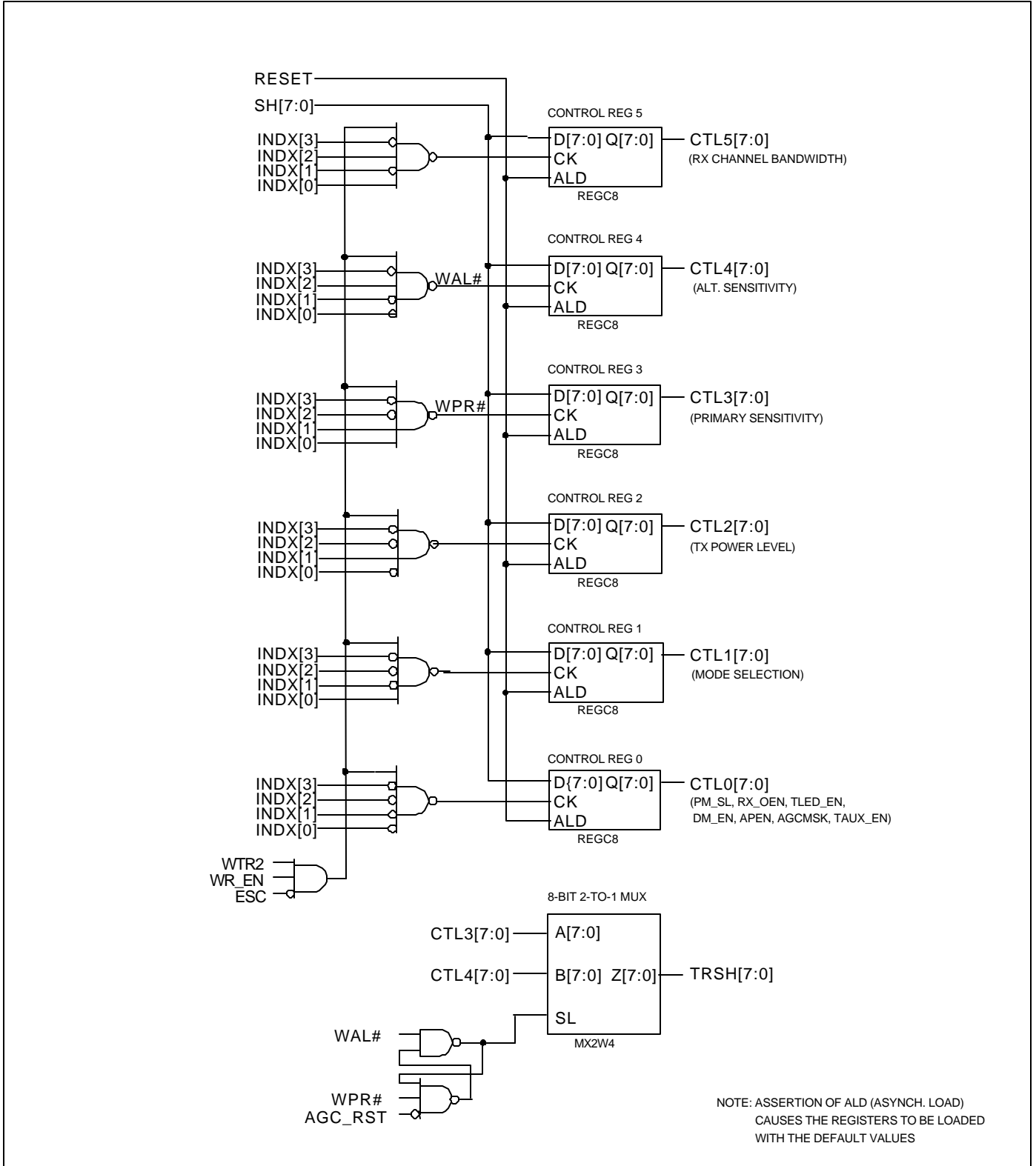


Figure A-2. Transceiver Control Registers

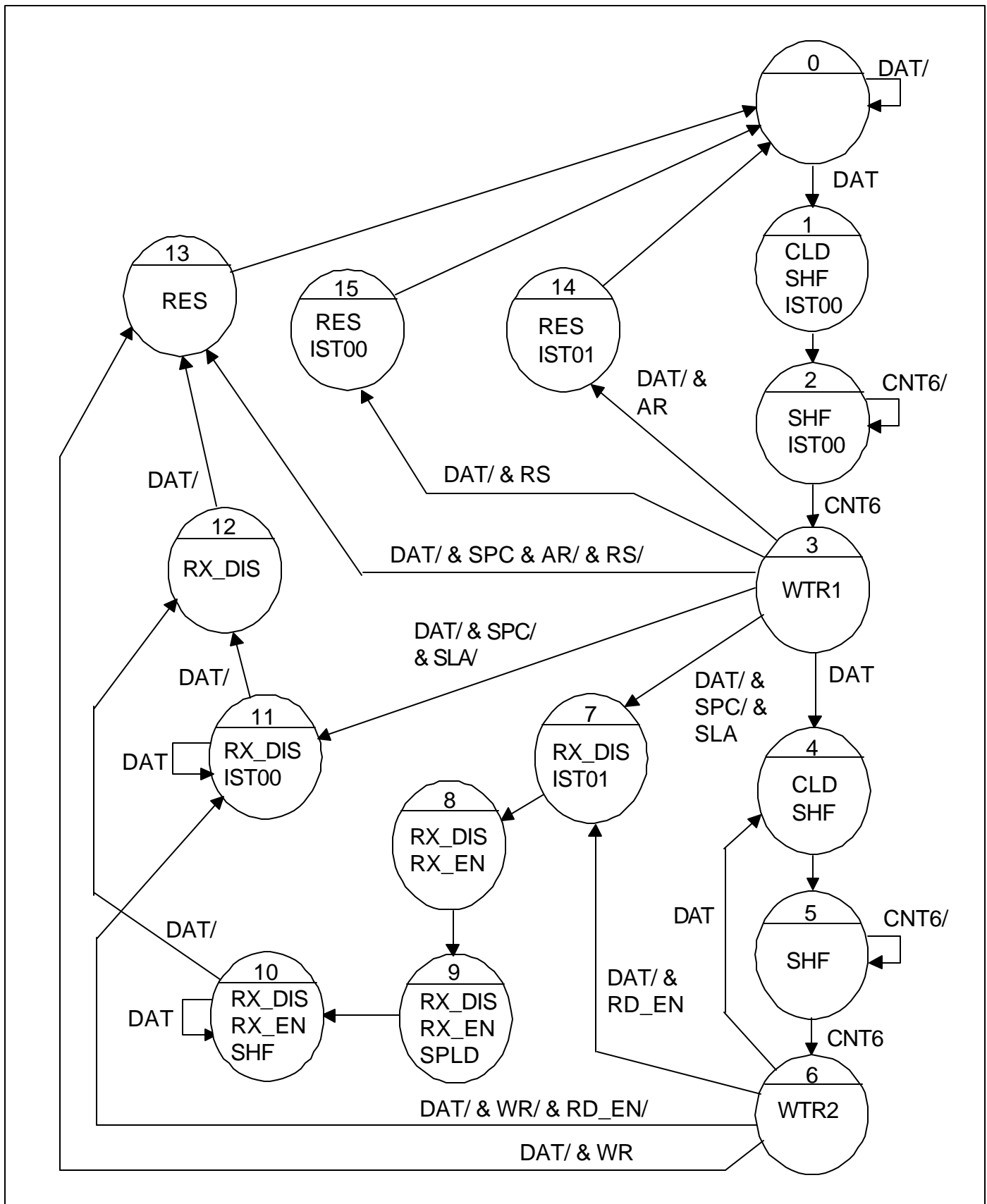


Figure A-3. Serial Interface State Diagram, (Slave Side)

APPENDIX B

Interconnecting two transceivers with the same address.

The following configuration allows two transceivers having the same fixed address to be used in a system. This configuration is not part of this specification and should only be considered as an interim solution since it is not expandable and does not support Plug-n-Play.

It is strongly recommended that future transceivers provide support for at least two selectable addresses.

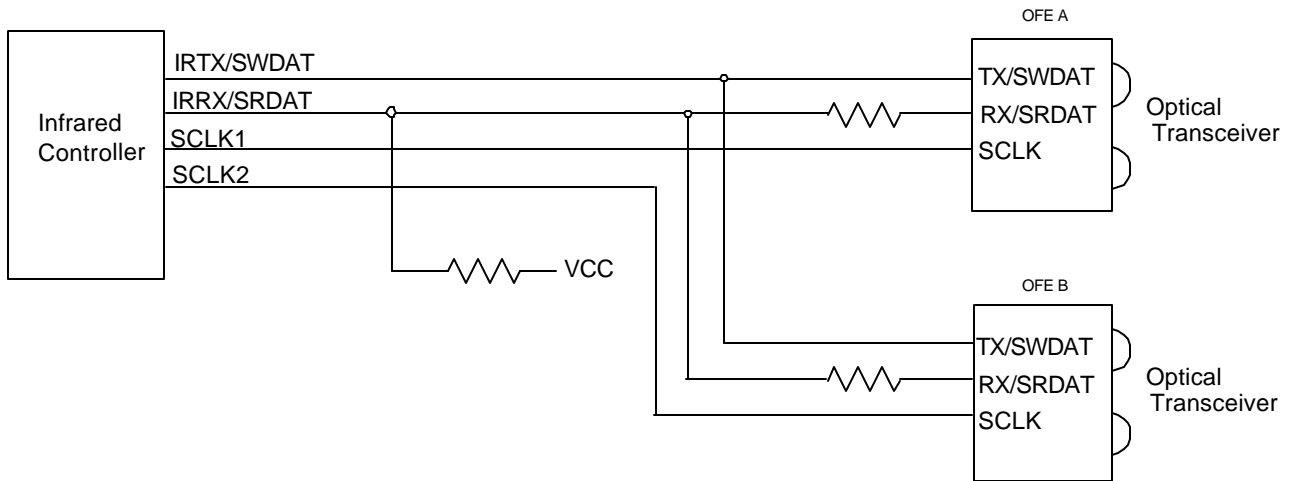


Figure B-1. Interface to Two Infrared Transceivers.

The data lines are multiplexed with the transmitter and receiver signals and separate clocks are used since the transceivers respond to the same address.