



Digital Semiconductor 21143 Connection to the Network Using Physical Layer Devices:

An Application Note

Order Number: EC-QXY7A-TE

This document provides the information necessary to implement the system and network connections to the Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller. The 21143 is a 10/100-Mb/s Ethernet-to-PCI controller. Other bus implementations can be made through the use of proper bus-to-bus interfaces.

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1 Implementing Network Connections

This application note provides a description of how to implement 100BASE-TX, 100BASE-T4, and 10BASE-T network connections using the Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (referred to as the 21143).

This document includes design recommendations and layout recommendations using media-independent interface (MII) based physical layer devices provided by Micro Linear, Integrated Circuit Systems, National Semiconductor, and Broadcom, and symbol (SYM) based physical layer devices provided by GEC Plessey and Quality Semiconductor. Throughout this document, a physical layer device is referred to as a PHY or PHY device.

Note: This application note does not describe the 21143 software interface. For more information on the software interface, refer to the *Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual*. (See Appendix B for ordering information.)

1.1 Functional Overview

This section provides an overview of the 21143 and the implementation of 100-Mb/s and 10-Mb/s network connections using MII-based or SYM-based PHY devices.

1.1.1 21143 Overview

The 21143 is a single-chip bus master Ethernet/Fast Ethernet device that supports direct memory access (DMA) and has direct interfaces to both the CardBus and the PCI local bus. The 21143 implements a direct interface to the CardBus or PCI bus through a single 50-pin connection, which consists of the control and address/data signals.

The 21143 provides a complete implementation of the IEEE 802.3 Ethernet specification. This includes the attachment unit interface (AUI), twisted-pair (10BASE-T) interface, MII SYM port interface, and the interface through the media access control (MAC) layer that creates a direct interface to the PCI bus.

The PCI interface utilizes only about 10% of the bus bandwidth during fully networked operation for 100-Mb/s Fast Ethernet reception or transmission. This bus master design results in high throughput between the system and the network.

1.1.2 Network Interface

The 21143 physical layer design supports AUI drop cable Ethernet and 10BASE-T twisted-pair (TP) Ethernet connections. The 21143 `gep<0>/aui_bnc` (pin 100), which is software controlled, provides for a connection of either the AUI (10BASE5) or BNC (10BASE2) network connector. Table 1 describes the function of this pin.

Table 1 Signal `gep<0>/aui_bnc` Description

Program State	Function
0	AUI port enabled; BNC port disabled.
1	BNC transceiver (or dc-to-dc converter) enabled; AUI port disabled

Functional Overview

AUI signals interface with the Manchester encoder/decoder portion of the 21143. The 21143 supports 10BASE5 thickwire and 10BASE2 ThinWire connections. The 10BASE2 connection requires an external transceiver.

The 21143 implements the 100BASE-T MII layer and the 100/10-Mb/s Ethernet MAC layer. The 21143 provides a dual network interface for both a 100BASE-T and a 10-Mb/s Ethernet. At the 100BASE-T port, the 21143 supports the industry-standard MII for any 100BASE-T implementation.

The 21143 is fully compliant with the MII specifications (as defined in IEEE 802.3). The MII is a nibblewide, general interface, that can be used with various physical interfaces, such as 100BASE-TX, 100BASE-T4, shielded twisted-pair (STP), and fiber. It also supports dual rates of speed (10 Mb/s and 100 Mb/s).

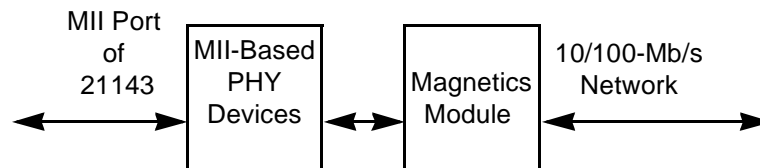
The 21143 includes special support for 100BASE-TX networks by including the PCS section (scrambler and 5B/4B coding/decoding). Integrating the 10BASE-T ENDEC with the 100-Mb/s-only SYM-based PHYs enables full support for a 10/100-implementation.

1.1.3 MII-Based PHY Block Diagram

Figure 1 is a block diagram of a 10BASE-T and 100BASE-T single-connector network connection using a MII-based PHY device with the 21143.

MII-based PHY devices are provided by Micro Linear, Integrated Circuit Systems, National Semiconductor, and Broadcom.

Figure 1 MII-Based PHY Design



The MII-based PHY design includes the following components:

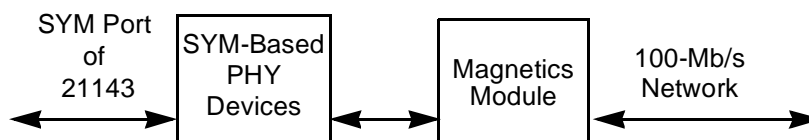
- The MII-based PHY devices, which have a direct interface to the MII port of the 21143 with dual-rate option (as specified in the MII specification) and a full interface to the 10/100-Mb/s magnetics module.
- The magnetics module, which is based on transformers and serial chokes enabling the network connection to the 100-Mb/s network (100BASE-TX or 100BASE-T4) and to the 10-Mb/s network (10BASE-T).

1.1.4 SYM-Based PHY Block Diagram

Figure 2 is a block diagram of a 100BASE-TX single-connector network connection using a SYM-based PHY device with the 21143. For a 10-Mb/s network connection, the network can be connected directly to the 21143 through filters and chokes.

SYM-based PHY devices are provided by GEC Plessey and Quality Semiconductor.

Figure 2 SYM-Based PHY Design



The SYM-based PHY design includes the following components:

- The SYM-based PHY devices, which have a direct interface to the SYM port of the 21143 with an interface to the 100-Mb/s magnetics module.
- The magnetics module, which is based on transformers and serial chokes enabling the network connection to the 100-Mb/s-only network (100BASE-TX or 100BASE-T4).

1.2 21143 Ports

Table 2 lists the active AUI signals when the 21143 AUI port is selected.

Table 2 AUI Signals

Signal	Pin Number
au _i _cd ₋	138
au _i _cd ₊	137
au _i _rd ₋	140
au _i _rd ₊	139
au _i _td ₋	143
au _i _td ₊	142

Table 3 lists the active twisted-pair signals when the 21143 10BASE-T port is selected.

Table 3 Twisted-Pair Signals

Signal	Pin Number
tp _{rd} ₋	10
tp _{rd} ₊	9
tp _{td} ₋	5
tp _{td} _{- -}	4
tp _{td} ₊	6
tp _{td} ₊ +	7

Table 4 lists the active MII signals when the 21143 MII port is selected.

Table 4 MII Signals

Signal	Pin Number
mii_clsn	118
mii_crs	117
mii_dv	129
mii_mdc	134
mii_mdio	135
mii_rclk	128
mii_rx_err	127
mii_rxd <3:0>	133:130
mii_tclk	124
mii_txd<3:0>	119:122
mii_txen	123

Table 5 lists the active SYM signals when the 21143 SYM port is selected.

Table 5 SYM Signals

Signal	Pin Number
sd	117
sel10_100	127
sym_rclk	128
sym_rxd<0>	130
sym_rxd<1>	131
sym_rxd<2>	132
sym_rxd<3>	133
sym_rxd<4>	118
sym_tclk	124
sym_txd<0>	122
sym_txd<1>	121
sym_txd<2>	120
sym_txd<3>	119
sym_txd<4>	123

1.3 Network Connection

The network connections of the 21143 can be used in 10BASE-T, AUI, MII, or SYM configurations. Different methods are used to connect each port to the actual cable connector.

1.3.1 10BASE-T Twisted-Pair Network Port

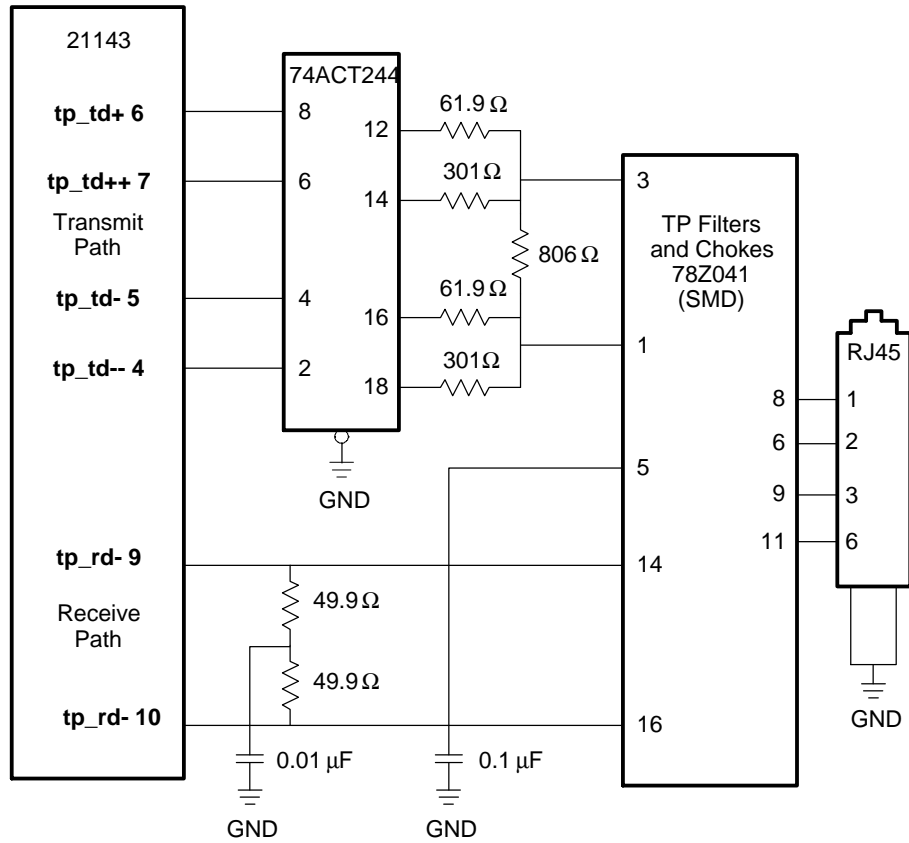
Figures 3, 4, and 5 show the network connection design options for 10BASE-T type implementations. Figures 3 and 4 show two ways of connecting the 10BASE-T network by using a standard 1:1 transformer module. This implementation type requires a swing compensator (to swing the 21143 output from 3.3 V to 5.0 V) to meet the standard requirements. Figure 5 shows a direct connection to a $1:\sqrt{2}$ transformer module. This implementation type provides the lowest component count for 10BASE-T. The filter and transformer components minimize any potential electromagnetic interference and radio frequency interface problems. Common-mode noise (when noise between two lines of the same polarity *add* rather than cancel) can radiate energy from the twisted-pair interface. Also, significant common-mode power supply noise can be generated on the board or adapter by other devices. Therefore, Digital Semiconductor recommends the use of filter and transformer modules that incorporate common-mode chokes.

Tables 8 and 9 list the part numbers for each implementation. Figure 3 shows the 10BASE-T network connection with buffers. The required components for this configuration are as follows:

- Voltage swing compensator — 74ACT244
- Terminating and decoupling components
- Filter transformer and common-mode chokes
- RJ45 connector

Network Connection

Figure 3 10BASE-T Network Connection with Buffers

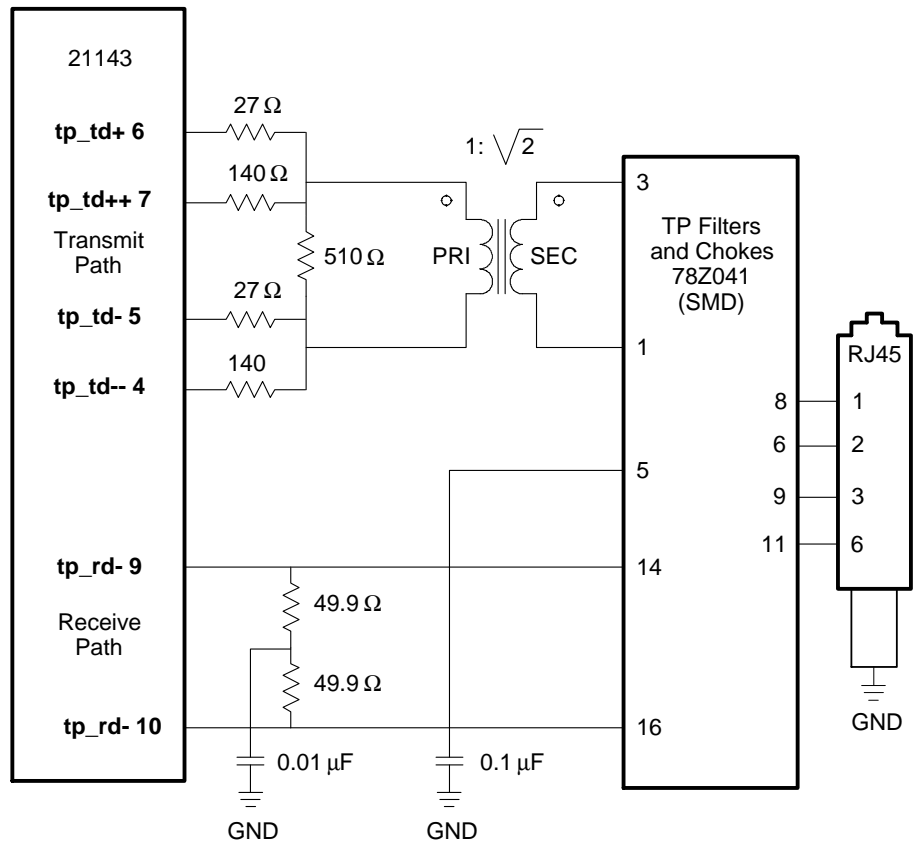


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Figure 4 shows the 10BASE-T network connection without buffers. The required components for this configuration are as follows:

- Terminating and decoupling components
- Transformer module (ratio of $1:\sqrt{2}$ for swing compensation)
- Filter transformer and common-mode chokes
- RJ45 connector

Figure 4 10BASE-T Network Connection Without Buffers



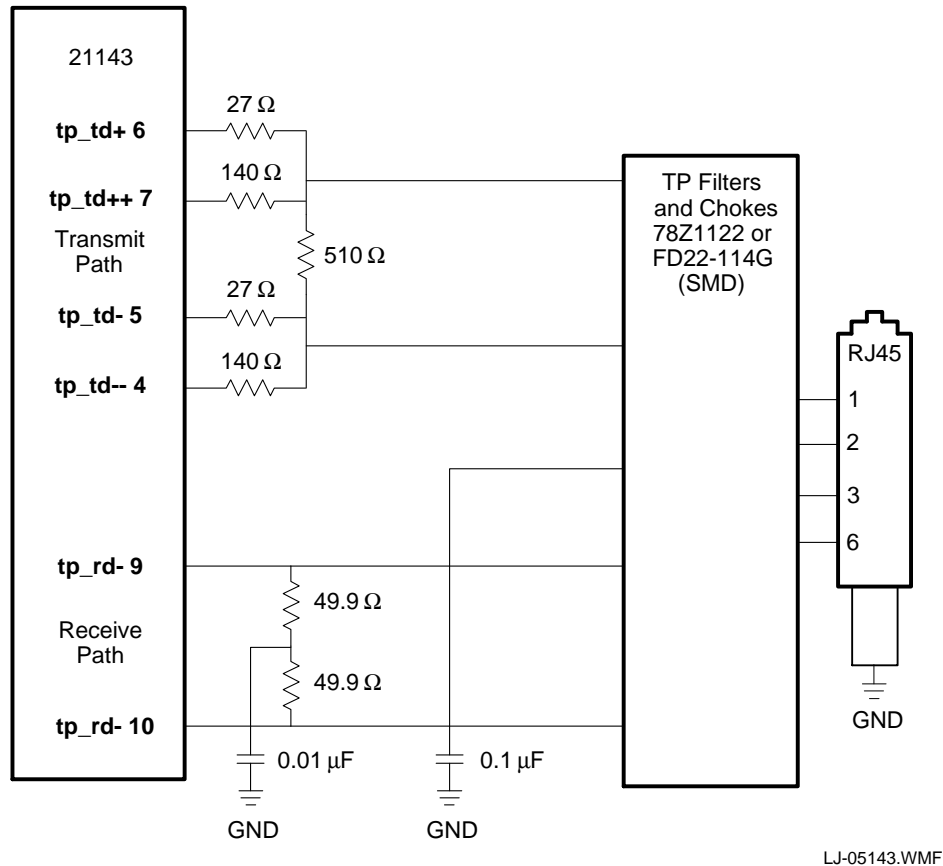
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Figure 5 shows the minimum component requirement for the 10BASE-T network connection. This implementation uses a filter transformer module with a $1:\sqrt{2}$ transformer on the transmit path to compensate for the voltage swing. The required components for this configuration are as follows:

- Terminating and decoupling components
- Filter, transformer, and common-mode chokes
- RJ45 connector

Network Connection

Figure 5 Minimum Components Required for 10BASE-T



1.3.2 100-Ready Designs

The 21143 can also be designed for systems that are “100-Ready.” The term “100-Ready” implies a system that has a 10-Mb/s network that can easily be upgraded to become a 10/100-Mb/s network. There are two methods for providing 100-Ready designs:

- Provide a connector for an internal optional daughtercard.
- Provide an MII connector for an external module that connects to the MII/SYM port.

These two methods are described in Table 6.

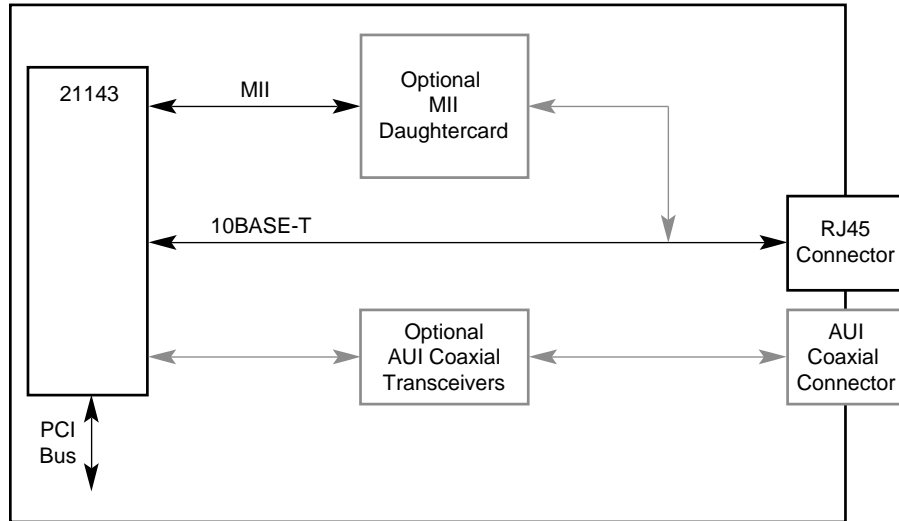
Table 6 Internal vs. External Design Features

Design	Features
Internal optional daughtercard	— Can be designed with an MII or any custom connector. — User opens cabinet to install 100-Mb/s daughtercard.
External MII/SYM module	— User connects module to external MII/SYM connector; user does not have to open cabinet for installation.

1.3.2.1 Internal Optional Daughtercard

Figure 6 shows a block diagram of a 100-Ready design using a daughtercard.

Figure 6 10BASE-T 100-Ready Daughtercard Block Diagram



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1.3.2.2 Description of 100-Ready Daughtercard Block Diagram

The blocks in the 10BASE-T 100-Ready block diagram represent the following components:

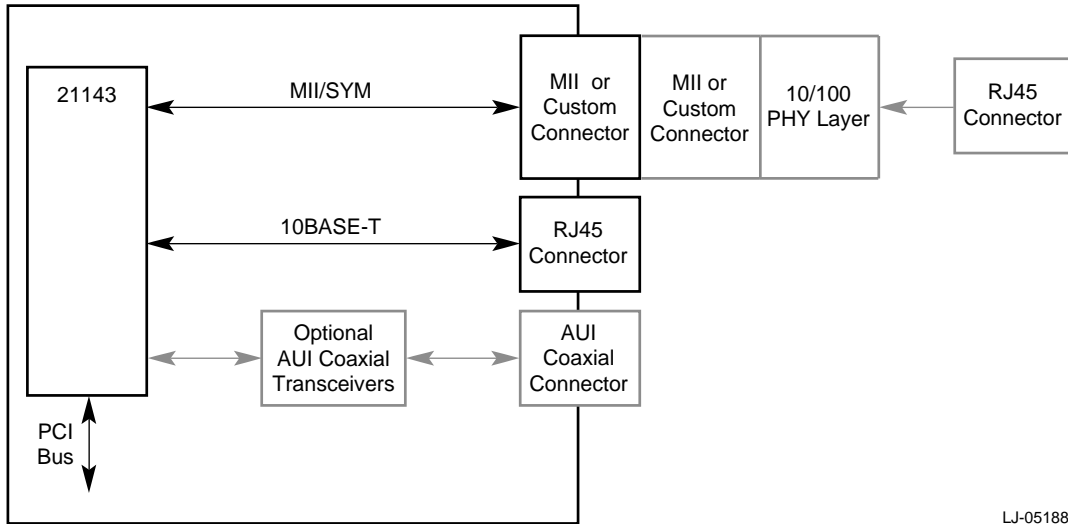
- 21143 — A 21143 with all of the external components for operating the network connection (reference parts, XTAL, and so on). The 21143 can use the PCI bus, and the MII/SYM, 10BASE-T, and AUI coaxial ports for communication.
- Optional MII/SYM daughtercard — A daughtercard with a 100-Mb/s or 10/100-Mb/s PHY that interfaces with an MII connector or custom connector. The daughtercard can be designed to use the same RJ45 connector.
- RJ45 — A network connection.

1.3.2.3 100-Ready External Module Design

Figure 7 shows a block diagram of a 100-Ready design using an external module.

Network Connection

Figure 7 10BASE-T 100-Ready External Module Block Diagram



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1.3.2.4 Description of 100-Ready External Module Block Diagram

The blocks in the 100-Ready external module block diagram represent the following components:

- 21143 — A 21143 with all of the external components for operating the network connection (reference parts, XTAL, and so on). The 21143 can use the PCI bus, and the MII/SYM, 10BASE-T, and AUI coaxial ports for communication.
- Optional external MII/SYM daughtercard — A daughtercard with a 100-Mb/s or 10/100-Mb/s PHY that interfaces with an MII connector or custom connector. The daughtercard uses the magnetics to connect to the RJ45 connector.
- MII connector — An MII or custom connector that connects with the MII/SYM port of the 21143.
- RJ45 — A network connection.

1.3.3 MII/SYM Pin Listing

Table 7 describes the MII/SYM pin multiplexing enabling the full flexibility for both network connections options using the same internal connector for the MII-based or the SYM-based PHY device (for detailed implementation notes, refer to the specific PHY device section in this document).

Table 7 MII/SYM Pinout

(Sheet 1 of 2)

Pin Number	MII Interface Function	SYM Interface Function
117	mii_crs	sd
118	mii_cls	sym_rxd<4>
119	mi_txd<3>	sym_txd<3>
120	mi_txd<2>	sym_txd<2>
121	mi_txd<1>	sym_txd<1>
122	mii_txd<0>	sym_txd<0>

Table 7 MII/SYM Pinout

(Sheet 2 of 2)

Pin Number	MII Interface Function	SYM Interface Function
123	mii_txen	sym_txd<4>
124	mii_tclk	sym_tclk
127	mii_rx_err	sel10_100
128	mii_rclk	mii_rclk
129	mii_dv	N.C.
130	mii_rxd<0>	sym_rxd<0>
131	mii_rxd<1>	sym_rxd<1>
132	mii_rxd<2>	sym_rxd<2>
133	mii_rxd<3>	sym_rxd<3>
134	mii_mdc	N.C.
135	mii_mdio	N.C.

1.3.4 AUI Network Port

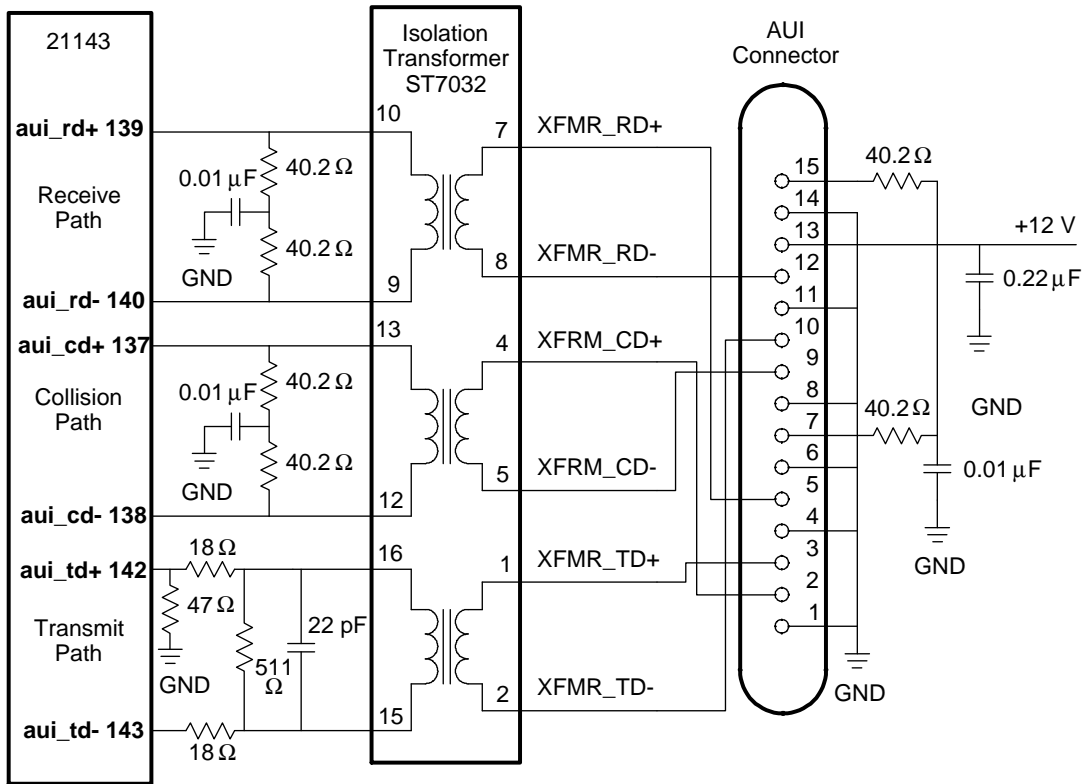
The 21143 is fully compliant with the AUI standard. The AUI can interface with an external medium-attachment unit (MAU) and connect to alternate media, such as 10BASE2 (ThinWire) and 10BASE5 (thickwire). Figures 8 and 9 show the required connections.

Figure 8 shows the AUI 10BASE5 network connection and the pin connections between the 21143 and the isolation transformer. The required components for this configuration are as follows:

- Terminating and decoupling components
- Isolation transformer
- AUI connector

Network Connection

Figure 8 AUI 10BASE5 Network and Pin Connections

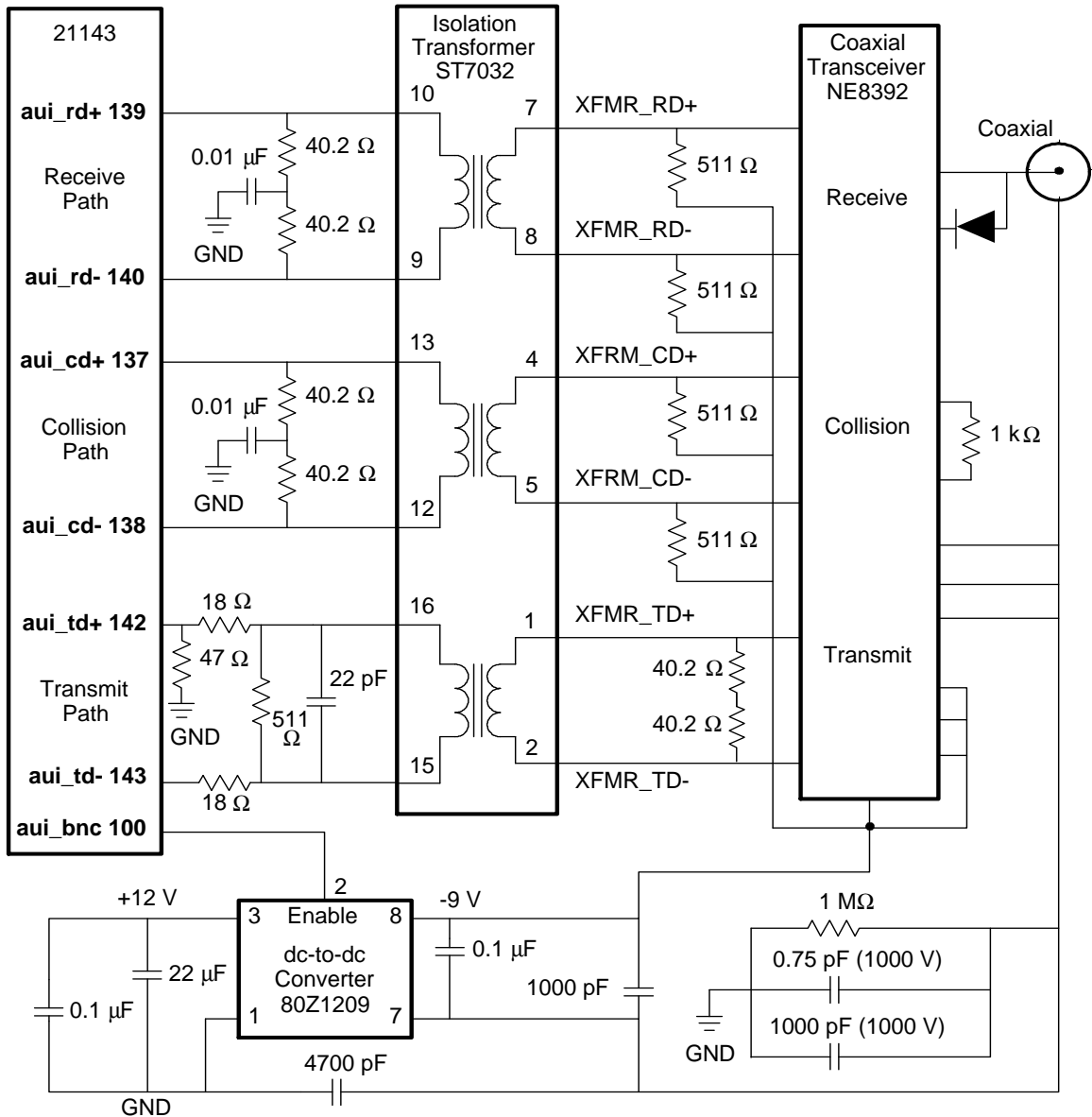


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Figure 9 shows the AUI 10BASE2 network connection. In this configuration, the AUI is not externally exposed. The required components for this configuration are as follows:

- Isolation transformer
- Terminating and decoupling components
- dc-to-dc converter
- Coaxial transceiver and BNC connector

Figure 9 AUI 10BASE2 Network Connection



Note:
Refer to the vendor data sheet for the specific implementation of the coaxial transceiver (NE8392).

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In cases where the 10BASE2 MAU is a module separate from the board, the MAU can be implemented on a small add-in card. Ensure that the cable used to connect the board to the MAU provides adequate shielding of the AUI signals from external noise. This MAU add-in card includes the following components:

- Transceiver chip and BNC connector
- dc-to-dc converter
- Discrete devices

Network Connection

1.3.5 Media-Specific Components

Table 8 lists the media-specific interface components for 10BASE-T access.
Table 9 lists the media-specific interface components for 10BASE2 and 10BASE5 access.

Table 8 10BASE-T Media-Specific Components

Access Type	Components	Available Part Numbers
10BASE-T	74ACT244 driver	74ACT244 or 74FCT244
	Filter and transformer module	Pulse Engineering PE65745 ¹ Valor PT4096 ¹ Valor ST7011 ¹ Halo TD42-2006Q ¹ Halo TG42-2006W1 ¹
	Transformer filter and chokes	Pulse Engineering PE65434 Valor FL1012
	RJ45 wire jack connector	—

Table 9 10BASE2 and 10BASE5 Media-Specific Components

Access Type	Components	Available Part Numbers
10BASE2	dc-to-dc converter	Fil Mag 80Z1209DSND
	Isolation transformer	Valor ST7032 ¹ Pulse Engineering PE65723 ¹ Valor LT6032 ¹ Valor ST6032/3 ¹ Halo TD01-0756K ¹ Halo TG01-0756W ¹
	Coaxial transceiver	National Semiconductor DP8392C
	Connector	—
10BASE5	Isolation transformer	Valor ST7032 ¹ Pulse Engineering PE65723 ¹ Valor LT6032 ¹ Valor ST6032/3 ¹ Halo TD01-0756K ¹ Halo TG01-0756W ¹
	AUI connector	—

¹Surface-mount device.

1.4 21143 Requirements

This section provides information about the external component connections for the 21143, and describes the following requirements:

- Unused JTAG port requirements
- Current reference and capacitor input
- Crystal connection or crystal oscillator connection for the serial clock connection

1.4.1 Unused JTAG Port Requirements

Table 10 describes the 21143 signal pin requirements if you are *not* using the JTAG port.

Table 10 Pin Requirements When Not Using the JTAG Port

Leave the Following JTAG Pins Open:		Pull the Following JTAG Pin Up or Down:	
tms (pin 1)		tck (pin 120)	
tdi (pin 2)			
tdo (pin 4)			

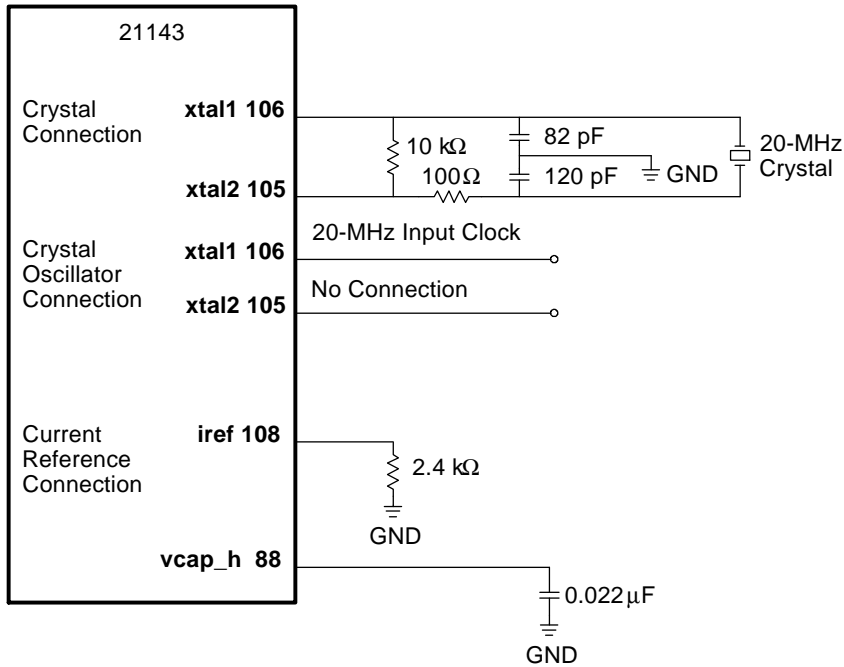
1.4.2 Current Reference and Capacitor Input Requirements

Table 11 describes the current reference and capacitor input requirements for the 21143, and Figure 10 shows the external component connections.

Table 11 Current Reference and Capacitor Inputs

Pin Name	Pin Number	Function	Connect This Pin...
iref	86	Current reference input for the analog phase-locked loop (PLL)	Through a 2.4-k Ω resistor to ground
vcap_h	88	Capacitor input	Through a 0.022- μ F capacitor to ground

Figure 10 21143 External Component Connections



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1.4.3 Crystal and Crystal Oscillator Connections

Figure 10 shows two serial clock connections; select either the crystal connection or the crystal oscillator connection. According to the IEEE 802.3 standard, a 20-MHz crystal is required. The crystal frequency must not vary by more than 100 parts per million (PPM), or 0.01%. Place the crystal as close as possible to the 21143.

Because the frequency of crystals from different vendors can vary, test the crystals in the actual circuit. It may be necessary to vary the tuning of the surrounding components. However, after the capacitors have been tuned for the specific crystal, the design does not need to be altered on a board-by-board basis.

The 21143 also supports a crystal oscillator (Figure 10). In this configuration, no external component is required and the **xtal2** pin should be left open. This is useful for applications with multiple network connections.

Table 12 lists the crystal specifications.

Table 12 Crystal Specifications

Specification	Value	Units
Crystal frequency	20.000	MHz
Frequency tolerance	±50	PPM
Load capacitance	50	pF
Frequency stability	±30	PPM
Maximum effective series resistance	40	Ohms (Ω)
Test condition drive level	100	μ W

1.5 Signal Routing and Placement

The Ethernet circuitry should be kept free of interference from unrelated signal traces. Routing for other signals must be kept away from the space surrounding the grouped Ethernet components. Place the Ethernet circuitry at the perimeter of the board, as close as possible to the network connector.

The onchip crystal oscillator requires an external crystal and discrete components. For stable and noise-free operation, place the crystal and discrete components as close as possible to the 21143, keeping the etch length as short as possible. Do not route any noisy signals in this area.

The PCI pin ordering is fully compatible with the PCI specification recommendation and can be easily routed within the specified etch limits of the PCI signals. This includes shared signal lengths of up to 3.8 cm (1.5 in) and the clock signal length of 6.41 cm (2.5 in).

Keep all signal paths short and route them as directly as possible.

Systems using the 10BASE-T nodes can be connected by cables up to 100 m (328 ft.). As a result, the signal that reaches the board can be noisy and low in amplitude. To minimize corrupting this data, route these signals, by the most direct path, from the network connector and through the magnetics coupler to the 21143.

The length of this path should not exceed 8 cm (3 in) for the active AUI signals. The MII/SYM interface operates at 25 MHz (or 2.5 MHz). All routing of the MII/SYM signals to the MII/SYM device should be as short as possible and should not have significant differences of lengths and characteristics within signal groups. Examples of signal groups include **mii_rxd<4:0>** and **mii_txd<4:0>**.

Note: The routing of these signals should be done with caution. The preferred routing of these signals is in the external routing layers of the board. The MII/SYM device should be located between the 21143 and the magnetics port.

1.5.1 Ground and Power Planes

Up to four types of power signals require handling when implementing a design with the 21143:

- **Gnd** is adapter ground.
- **Vcc** (+5 V from PCI) drives the external components (boot ROM and Ethernet address ROM).
- **Vdd** (+3.3 V) drives the 21143.
- **Vee** (-9 V output) power from the dc-to-dc converter if the coaxial network connection is implemented. For information specific to the -9 V power supply, refer to the transceiver used to drive the coaxial network connection.

Digital Semiconductor recommends that at least two power planes be kept on the PCB: **Vcc** and **Gnd**. The **Vdd** power plane (+3.3 V) can be implemented either by a cut in the **Vcc** power plane, or by a power island under the 21143 on one of the signal routing layers.

Signal Routing and Placement

Digital Semiconductor recommends that decoupling capacitors should be connected to all power supplies. These capacitors should be placed as close as possible to the power pins of the chips. The recommended values are as follows: 0.1 μF , 0.01 μF , 10 μF (tantalum), and 47 μF (tantalum).

For better noise-testing immunity, separate all power planes between the network connectors and the transformer from the logic and analog power planes of the adapter for the 10BASE-T, 10BASE2, 100BASE-T4, and 100BASE-TX connections.

Digital Semiconductor also recommends that the connector's shield of the adapter should be connected to the PC chassis.

1.5.1.1 3.3-V Power Supply

The 21143 operates with a power supply of 3.3 V. At least eight decoupling capacitors are recommended and should contain the following values:

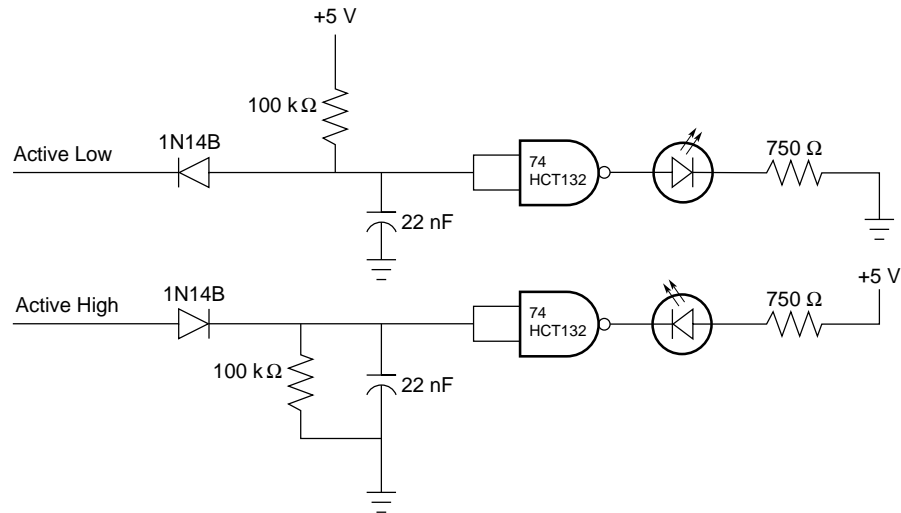
- Three each at 0.1 μF
- Three each at 0.01 μF
- One each at 10 μF (tantalum)
- One each at 47 μF (tantalum)

1.5.2 LED Status Signals

The LED connection requires a series resistor that is connected to ground. This resistor value should be calculated according to the type of LED used. A typical 2-mA LED requires a 750- Ω resistor. For implementations using the boot ROM, the LED current should not exceed 2 mA. For LED indication and programming information, refer to the CSR15 definition in the *Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual*.

The 21143 requires LED time-stretching logic for a visible indication of the activity signal. Figure 11 shows how to implement this circuit.

Figure 11 LED Time-Stretcher Circuit



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1.6 Design Considerations

This section provides information to aid the user in designing Ethernet and Fast Ethernet capabilities onto a motherboard. In addition, it also includes design considerations for FCC compliance.

1.6.1 Designing the Ethernet Corner on Motherboards

This subsection provides a list of routing suggestions and a list of component placement suggestions.

The following list contains routing recommendations:

- Minimize the length of high-frequency signals.
- Route differential signal pairs together.
- Minimize the use of vias for high-frequency signals.

The following list contains component placement recommendations.

- Refer to the *PCI Local Bus Specification, Revision 2.1* for the placement of the 21143 with relation to the PCI bus.
- Place the 21143 as close to the PHY device as possible.
- Place the PHY device as close to the filters and magnetics as possible.
- Place the filters and magnetics as close to the RJ45 connector as possible.

1.6.2 Suggestions for FCC Compliance

Product designs and their associated applications are unique. Therefore, the designer must consider the total system or module implementation when determining a product design for FCC compliance.

Design Considerations

The following information is provided as suggestions only to aid the designer in meeting FCC regulations.

1.6.2.1 Suggestions for Quiet Ground and Power Planes

For quiet ground and power planes, consider the following suggestions:

- Isolate power plane for PLL stability and noise isolation of audio digital-analog converters and amplifiers.
- Partition ground planes to isolate the I/O from common system noise. Do not route any etch across an isolated or partitioned ground plane.

Note : Ground plane splits can affect a signal's return path back to its source. If the signal return path is along the ground plane underneath the signal etch, any interruption in the ground plane increases the return path loop area, which in turn, increases its ability to radiate.

- Add common-mode chokes to the design at the output of the isolation transformer to isolate the I/O from common system noise.
- Place high-speed signals between power and ground planes to reduce board-level radiation.

The following books are recommended as additional references:

- *Fundamentals of Electromagnetic Capability*, by William G. Duff
- *Engineering Electromagnetic Capability*, by V. Prasad Kodali

1.6.2.2 Suggestions for Routing

For routing information, consider the following suggestions:

- Never route any etch (power or ground) across a partition or void because the signal loses its return-path integrity and contaminates the isolated plane.
- Avoid placing oscillators, phase-locked loops, and other clock-type devices near I/O connectors.
- Route all critical signals (for example; clocks, video output) directly in the etch and avoid, if possible, using vias (signal paths routed between planes in an etch board).

Note: Critical signals should be prioritized from the fastest to the slowest with respect to frequency and rise time. The fastest critical signals should be routed first.

2 ML6692 MII PHY Network Implementation

This section describes the design of a 10/100-Mb/s network interface card with autonegotiation using the 21143 and the ML6692 100BASE-TX PHY device from Micro Linear.

2.1 ML6692 Overview

The functions between the MAC layer and the medium is called the PHY. The PHY contains all the coding, timing, and media transceivers to connect to the physical network. The ML6692 PHY device supports 100BASE-TX PHY-type functions, autonegotiation capability, and an analog buffer for 10BASE-T functions. These features permit the designer to use the 10BASE-T functions of the 21143 in conjunction with the 100BASE-TX functions and the autonegotiation capability of the ML6692, while still maintaining a single jack connection to the network.

The interface between the 21143 and the ML6692 is a mix of digital and analog signals. The 21143 contains the following features:

- A PCI interface
- 10/100-Mb/s MAC functions
- A media-independent interface (MII)
- An unfiltered 10BASE-T transceiver

The ML6692 is a 100BASE-TX PHY device that contains the following features:

- All circuits from the MII to the 100BASE-TX transceiver
- A times 10 analog buffer for 10BASE-T transmit signals (it drives the same pins as the 100BASE-TX transceiver for ease of output design)

2.1.1 MII Interface

The 21143 MII connects to the ML6692 interface for 100BASE-TX operation. The 21143 10BASE-T transceiver connects through a filter to the ML6692 analog buffer input for 10BASE-T operation.

The ML6692 100BASE-TX functions are accessible through its MII. Table 13 lists the transmit signals that pass through the transmit subset of the MII, and Table 14 lists the receive signals that pass through the receive subset of the MII.

Table 13 ML6692 Transmit Signal Functions

Transmit Signal	Function
TXCLKOUT	transmit clock out
TXEN	transmit enable
TXERR	transmit error
TXD<3:0>	transmit data bits 0 through 3

ML6692 Block Diagram

Table 14 ML6692 Receive Signal Functions

Receive Signal	Function
rxclk	receive clock
rxen	receive enable
rxerr	receive error
rxd<3:0>	receive data bits 0 through 3

2.1.2 Register Control

The ML6692 supports all of the IEEE 802.3 defined management registers that are accessed by management data clock (MDCLK) and management data input/output (MDIO) port. Through the management port, the registers can be written for control using restart autonegotiation, or read for status using link partner capability.

2.1.3 Filtering the Transmit Signal

The 10BASE-T transmit signal from the 21143 should be filtered and attenuated before it is transmitted by the ML6692 during 10BASE-T operation. When packets are received, the 21143 signals the ML6692 to keep the PHY device in 10BASE-T mode during heavy network activity. The 10BASE-T receive signals are routed through an analog switch and a filter to the 21143 10BASE-T receive inputs. When in the 100BASE-TX operation mode, the 10BASE-T filter is switched out by the analog switch.

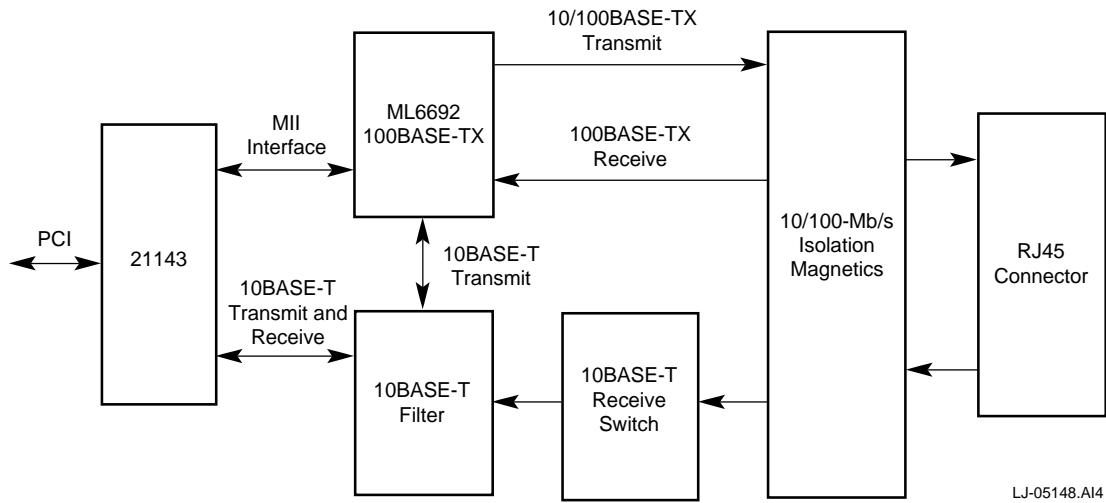
2.2 ML6692 Block Diagram

Figure 12 shows a block diagram of the ML6692. It incorporates the following components and capabilities:

- 21143
- ML6692
- 10BASE-T filter
- Receive switch
- A 10/100-Mb/s magnetics module consisting of transformers and series common-mode chokes to enable connection to either the 100-Mb/s network for 100BASE-TX operation, or the 10-Mb/s network for 10BASE-T operation.

Note: The 21143 10BASE-T transmit signal is routed through the times 10 analog buffer of the ML6692 for a connection to the 10/100-Mb/s magnetics module.

Figure 12 ML6692 Block Diagram

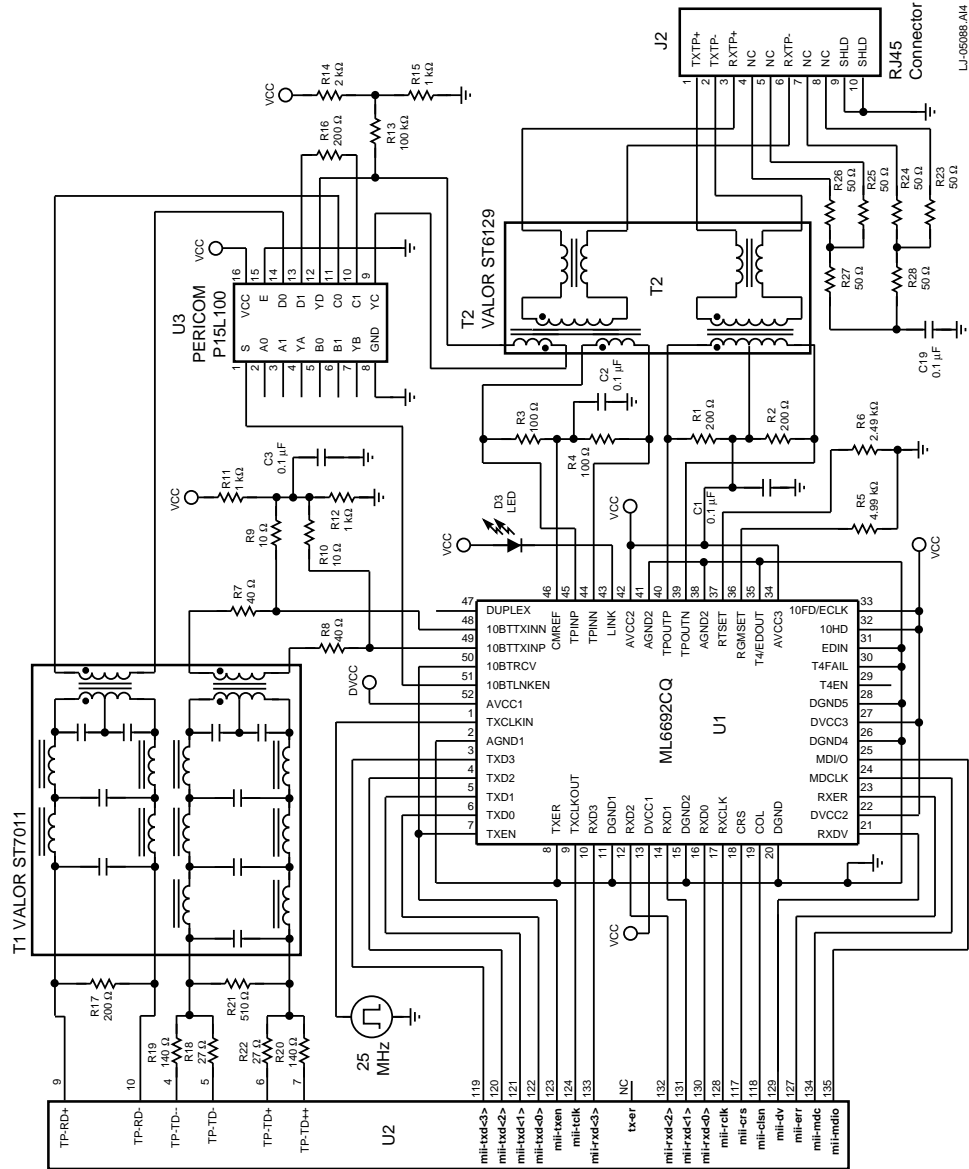


2.3 ML6692 Schematic Diagram Description

Figure 13 shows a schematic diagram of the ML6692 and Table 15 lists the components used. The schematic description that follows is segmented into 100BASE-TX transmit and receive operations, and 10BASE-T transmit and receive operations.

ML6692 Schematic Diagram Description

Figure 13 ML6692 Schematic Diagram



2.3.1 ML6692 Parts List

Table 15 lists the components used with the ML6692 in Figure 13.

Table 15 ML6692 Component Listing

(Sheet 1 of 2)

Component	Designator	Description	Comments
Resistors	R1, R2	200 Ω, 1/8 W, 1%	Source impedance
Resistors	R3, R4	100 Ω, 1/8 W, 1%	Termination impedance
Resistor	R5	4.99 kΩ, 1/8 W, 1%	Equalizer set
Resistor	R6	2.49 kΩ, 1/8 W, 1%	Amplitude set

Table 15 ML6692 Component Listing

(Sheet 2 of 2)

Component	Designator	Description	Comments
Resistors	R7, R8	40 Ω , 1/8 W, 1%	Termination impedance
Resistors	R9, R10	10 Ω , 1/8 W, 1%	Termination impedance
Resistors	R11, R12	1 k Ω , 1/8 W, 1%	Voltage bias
Resistor	R13	100 k Ω , 1/8 W, 5%	Voltage bias
Resistor	R14	2 k Ω , 1/8 W, 5%	Voltage bias
Resistor	R15	1 k Ω , 1/8 W, 5%	Voltage bias
Resistors	R16, R17	200 Ω , 1/8 W, 1%	Termination
Resistors	R18, R22	27 Ω , 1/8 W, 1%	Pre-emphasis
Resistors	R19, R20	140 Ω , 1/8 W, 1%	Pre-emphasis
Resistor	R21	510 Ω , 1/8 W, 1%	Pre-emphasis
Resistors	R23 through R28	50 Ω , 1/8 W, 5%	Optional (unused UTP termination)
PHY device	U1	ML6692CQ	100BASE-TX
IC	U2	21143	10/100-Mb/s MAC
Switch	U3	P15L100 Pericom LAN	10BASE-T switch
Transformer	T1	Valor ST7011	10BASE-T filter
Transformer	T2	Valor ST6129 or Bel Fuse S558-1287-01	10/100-Mb/s isolation module
Indicator	D3	LED	Link indication
Capacitors	C1 through C3	0.1 μ F, NPO, 20%	Bypass

2.3.2 100BASE-TX Transmit Operation

In 100BASE-TX operation, the MII signals from the 21143 connect to the corresponding pins of the ML6692. ML6692, pin 8, transmit error (TXER) is not used and should be grounded. All accesses to the 100BASE-TX functions are through the MII. No termination of the MII is required. The ML6692 MII outputs are series terminated with 68 Ω . The transmit data is encoded, scrambled, retimed, and then transmitted onto the unshielded twisted-pair. The current drive outputs (pins 39 and 40) are open-collector devices that pull current through the transformer while transmitting. The single-ended signal level should be 2 V peak-to-peak before it is stepped down, 2:1 by an isolation transformer. Because the output is stepped down 2:1, the source impedance decreases by a factor of 4, so pull-up resistors R1 and R2 are 200 Ω (usually, when the output is designed for a 1:1 isolation transformer, R1 and R2 would be 50 Ω). The RTSET resistor R6 is used to set the transmit amplitude with the selected isolation transformer T2.

ML6692 Schematic Diagram Description

2.3.3 100BASE-TX Receive Operation

The receive path is split into two paths at the isolation transformer. One path is routed to the 10BASE-T receive, and the other path is routed to the 100BASE-TX receive. When the receive path splits, the termination impedance also splits. Each path is a 200- Ω path so the parallel impedance is 100 Ω . Termination resistors R4 and R3 are 100 Ω each for this reason. The RGMSET resistor R5 is used to set the equalization threshold for the 100BASE-TX receive path. The design value for R5 is 5 k Ω . The **CMREF** pin generates the common-mode reference voltage of 3.82 V to properly bias the receive inputs for operation. When the input receives a **MLT3** signal, the signal pin **LINK** goes low sinking 5 mA of current through the LED. No series resistance is required.

2.3.4 10BASE-T Transmit Operation

In 100BASE-T transmit operation, the transmit path consists of the following components:

- Pre-emphasis resistors
- Transmit filter
- Resistor attenuator
- Common-mode bias generator

Since the 10BASE-T output of the 21143 is unfiltered, the transmit signals must pass through a transmit filter prior to being amplified by the ML6692 analog buffer. The single-ended 10BASE-T input to the ML6692 must have a swing of 500 mV peak-to-peak, and also a common-mode bias of $V_{cc}/2$. The ML6692 amplifies the transmit signal by a factor of 10, and then with isolation transformers, steps it down by a factor of 2. The resultant output is an IEEE 802.3 10BASE-T standard compliant signal of 2.5 V peak-to-peak, single-ended divided by a 5 V peak-to-peak, differential output from the RJ45 connector.

2.3.5 10BASE-T Receive Operation

In 100BASE-T receive operation, the receive path requires a receive filter. However, the 10BASE-T filter causes an impedance mismatch for 100BASE-TX signals, so it must be switched out when 100BASE-TX operation is selected. This is accomplished by using a Pericom P15L100 LAN switch that is controlled by the **10BTLNKEN** (pin 51) signal of the ML6692. The proper 100BASE-TX termination of the 10BASE-T filter and termination combination is automatically switched by the ML6692 either when autonegotiation is complete, or when the protocol speed is forced by the management interface. The 10BASE-T control interface signal consists of the 21143 transmit enable (**mii_txen**) to pin 50 of the ML6692 (10BTRCV). The 21143 drives the **mii_txen** to indicate to the ML6692 that the 10BASE-T packets have been received. The ML6692 contains a link pulse detector to detect link pulses. When packets are not being received, the ML6692 stays in 10BASE-T mode as long as link pulses are present on the receive pair.

2.4 ML6692 Layout Considerations

The most important consideration for the designer is the board layout. The board layout determines the board analog performance and electromagnetic (EM) emissions.

2.4.1 Choosing a Printed Circuit Board

The best printed circuit board (PCB) for the ML6692 is a multilayered PCB. A four-layer board, with two-ounce copper power planes, minimizes switching transients by providing a low-impedance power source. Creating an ideal power source is the goal when laying out power planes. With this in mind, it is preferable to combine both the 21143 and analog power supplies of the ML6692 into a common low-impedance supply. The use of split planes can be advantageous, but in a small form-factor design, this advantage is lost because the planes cannot be made large enough to be effective.

2.4.2 Minimizing Noise

Liberal usage of capacitors on the 21143 power pins minimizes any noise that may be coupled into the power plane. Power supply noise contributes to EM emissions in circuit layouts. EM emissions are reduced by many orders of magnitude when the 21143 switching-intensive MII is turned off. It is imperative, that low ESR capacitors with multiple-via connections to the power and ground planes be placed in close proximity to all power pins. Each capacitor should have at least two vias connecting the capacitor to the power plane, and two vias connecting the capacitor to the ground plane. These extra vias improve capacitor performance.

2.4.3 Lowering EM Emissions

The power and ground planes should extend underneath both the ML6692 and the bypass capacitors. The power and ground planes should not extend under any network signal path (the twisted-pair transmit and receive lines located between the ML6692 and the RJ45 connector), because common-mode power supply noise will be coupled to the network signals causing them to act like radiating antennae. Therefore, the design goal is to provide low-impedance power and ground planes around the ML6692 power and ground pins, while removing all grounds away from the network signal paths. The greater the distance between the power plane and the network signal paths, the lower the EM emissions. Route the 10BASE-T signal paths between the 21143 and the ML6692 away from the power and ground planes.

The emission frequencies of the ML6692 are usually in 25-MHz harmonics because the system clock operates at a speed of 25 MHz. Emission frequencies can be as high as 250 MHz. A stray capacitance of 5 pF has an impedance of 127 Ω at 250 MHz. This impedance determines how much current flows when the power noise couples to the network signal paths. The current, in turn, determines how much of the 250-MHz component is irradiated. So, to reduce irradiated noise, minimize stray capacitance.

2.4.4 Redirecting Common-Mode Noise into the Chassis

Use the chassis of the instrument where the adapter is installed to allow coupled noise to flow to ground. The chassis is not a perfect ground, but with proper instrument power supply design, the chassis can be used to redirect common-mode noise. The object is to surround the network signals on the RJ45 connector side of the isolation transformer

ML6692 Summary

with a chassis ground plane. The small coupling of the network signals to the chassis help attenuate the common-mode noise before leaving the chassis. This layout technique is called *stripline*. As with network signal paths, the farther power and ground planes are away from the chassis, the lower the EM emissions.

2.5 ML6692 Summary

This section provided the designer with sufficient information to design the physical connections between the 21143 and the ML6692. An adapter card can use the 10BASE-T functions of the 21143 and the 100BASE-TX functions and autonegotiation capabilities of the ML6692. With proper power supply layout, this circuit can pass CISPR“B” emission limits with a four-layer PCB.

3 ICS1890 MII PHYceiver Network Implementation

The ICS1890 PHYceiver integrates all physical layer functions of the IEEE 802.3 10BASE-T and 10BASE-TX from the MII to the isolation transformer of the 10/100-Mb/s magnetics module. This device allows system designers to implement the entire 10/100-Mb/s physical layer channel with one chip, using five passive components to support the onchip analog circuitry, while keeping the total power consumption under one watt. This section describes how to implement a 10/100-Mb/s adapter using the 21143 and the ICS1890.

3.1 ICS1890 Overview

The ICS1890 incorporates an MII 5-bit symbol interface, allowing easy connection to Digital Semiconductor's MAC layer. The interface operates in IEEE standard MII mode for both 10BASE-T and 100BASE-TX.

The ICS1890 employs autonegotiation logic that has three main features.

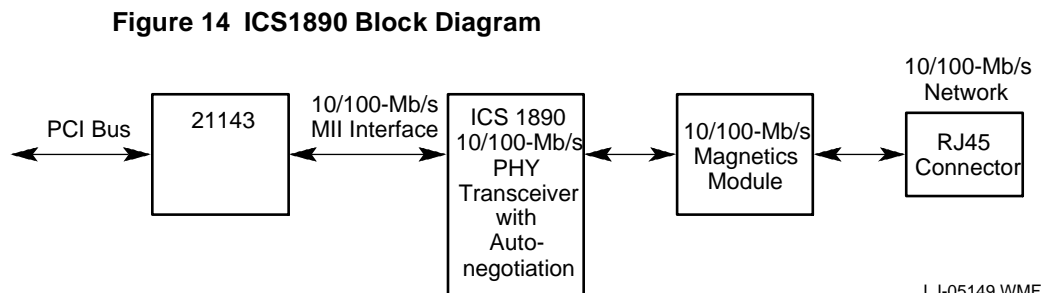
- Determines the capabilities of the remote link partner
- Advertises its own capabilities to the remote link partner
- Automatically adjusts to the highest performance common operating mode

The ICS1890 autonegotiation logic is designed to operate with legacy 10BASE-T networks or newer systems with multiple connection technology options. When operating with a legacy 10BASE-T remote partner, the ICS1890 selects the 10BASE-T operating mode transparent to the remote partner. This allows the preservation of existing legacy network structures without management intervention. Legacy 100BASE-TX devices that do not support autonegotiation are also identified and handled by the ICS1890.

3.2 ICS1890 Block Diagram

Figure 14 shows the physical layer design for the 10BASE-T and 100BASE-TX ICS1890 single-chip implementation and standard MII interface to the 21143 MAC.

The ICS1890 implements a fully compliant IEEE 802.3 MII for connection to MACs or repeaters. This allows connection between the ICS1890 and MAC either on the same board, on a motherboard/daughtercard, or through a cable in a similar manner to the AUI connections



3.3 ICS1890 Schematic Diagram Description

This section provides a schematic description of the implementation of a complete 10/100-Mb/s physical layer transceiver application from the MII to the RJ45 connector (using the ICS1890). It also provides an external component listing and information for selecting a 10/100-Mb/s magnetics module for the ICS1890 PHY device.

3.3.1 External Component Requirements

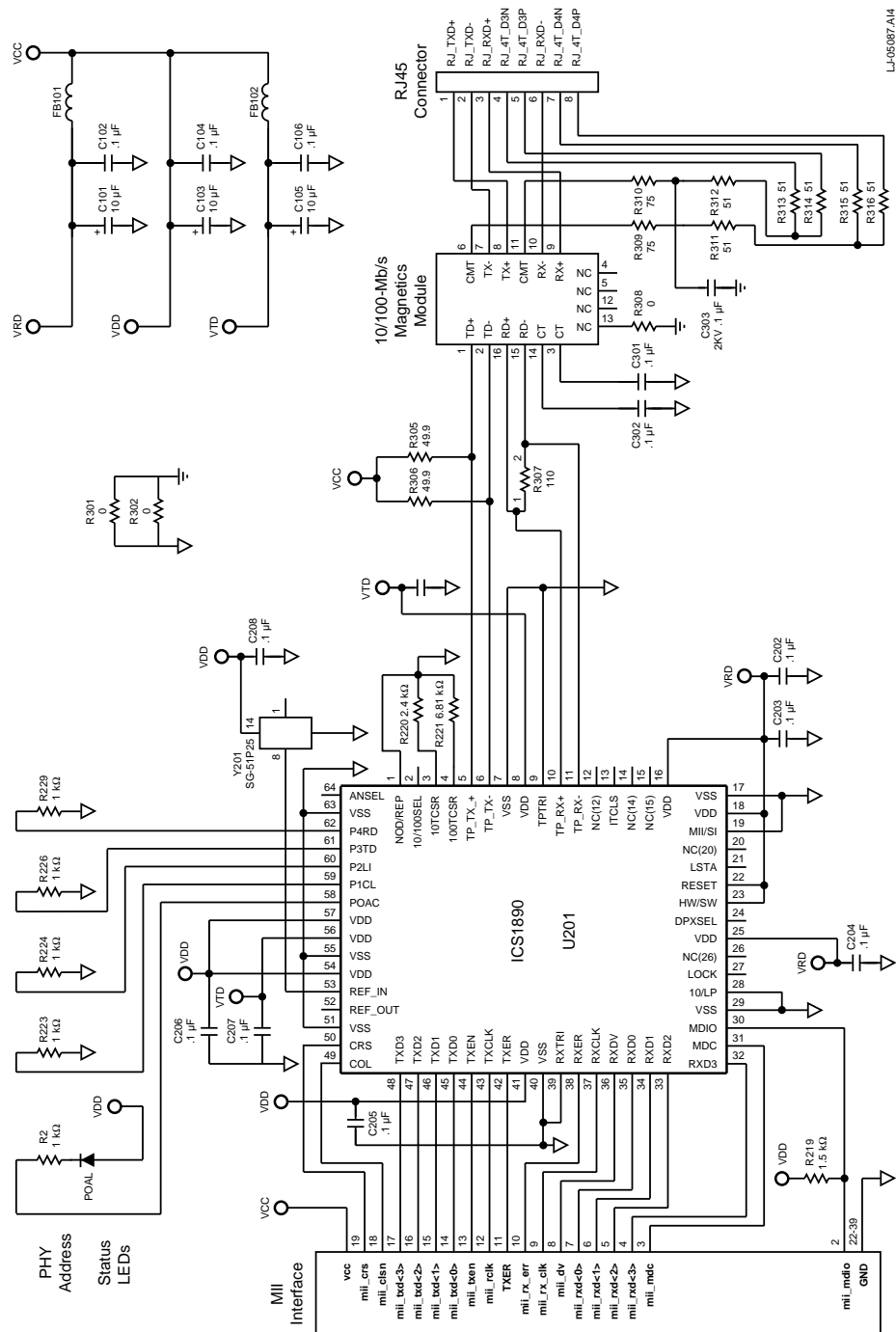
The ICS1890 connects directly to the MII and requires only five additional passive components to set transmit currents and match impedances. In addition, the design is comprised of the following components:

- 25-MHz clock oscillator
- MII PHY address LED or resistor
- Off-the-shelf, 10/100-Mb/s magnetics module
- Unused pair of termination resistors
- Normal bypass and decoupling capacitors

3.3.2 Schematic Information

Figure 15 shows detailed schematic information for the ICS1890 PHY device.

Figure 15 ICS1890 Schematic Diagram



3.3.3 External Component Listing

Table 16 lists the external components used with the ICS1890 in Figure 15. Only five resistors are required for the analog circuitry build. Two of the resistors are used to precisely set the transmit currents for 10BASE-T and 100BASE-TX. The remaining

ICS1890 Schematic Diagram Description

three resistors are used to match the impedance of the twisted-pair cabling. Other components are used optionally to enhance system design when using an MII connector or multiple LED indicators.

Table 16 ICS1890 External Components

Component	Description	Qty	Comments
Resistor	2.4 k Ω , 1/2 W, 1%	1	10BASE-T transmit current setting
Resistors	49.9 Ω , 1/2 W, 1%	2	Impedance matching
Resistor	110 Ω , 1/2 W, 1%	1	Impedance matching
Resistors ¹	51 Ω , 1/2 W	6	Unused twisted-pair terminations (for termination if desired)
Resistors ¹	75 Ω , 1/2 W	2	Unused twisted-pair terminations (for termination if desired)
Resistor	6.81 k Ω , 1/2 W, 1%	1	100BASE-TX transmit current setting
Resistor ¹	1.5 k Ω , 1/2 W	1	MDIO pull-up, optional if internal to the MAC
Resistors ¹	1 k Ω , 1/2 W	5	For LEDs (nominal range 510 Ω to 10 k Ω , 1/2 W)
Capacitors	0.1 μ F	14	For supply bypass
Capacitors	10 μ F	3	For supply decoupling
LED ¹	—	1	—
Ferrite beads or inductors	—	2	21143 and transmit/receive isolation
10/100-Mb/s magnetics module	—	1	Section 3.3.4 provides recommendations
Oscillator ¹	25 MHz, \pm 50 PPM	1	Values true for all conditions. A frequency reference with the same performance can also be substituted
RJ45 connector	—	1	Network connection

¹Component(s) not required for all system designs.

3.3.4 10/100-Mb/s Magnetics Module Selection

Table 17 lists some of the vendor magnetic modules that are compatible with the ICS1890 10/100-Mb/s, twisted-pair, PHY transceiver. These modules are off-the-shelf type modules designed for use with 10/100-Mb/s Ethernet devices.

Two configuration styles are available:

- No choke style
- Extra choke style

The no choke style in Figure 17 has an exposed center tap on the transmit side, therefore, it does not have a primary side common-mode choke.

The extra choke style adds a common-mode choke to the primary of the transmit side. This is possible because the ICS1890 drives the transmitter 1:1 for both 10BASE-T and 100BASE-TX.

Table 17 lists the vendors that provide pin-compatible modules using the no choke style and the extra choke style transformers. Some vendors offer more than one type of module.

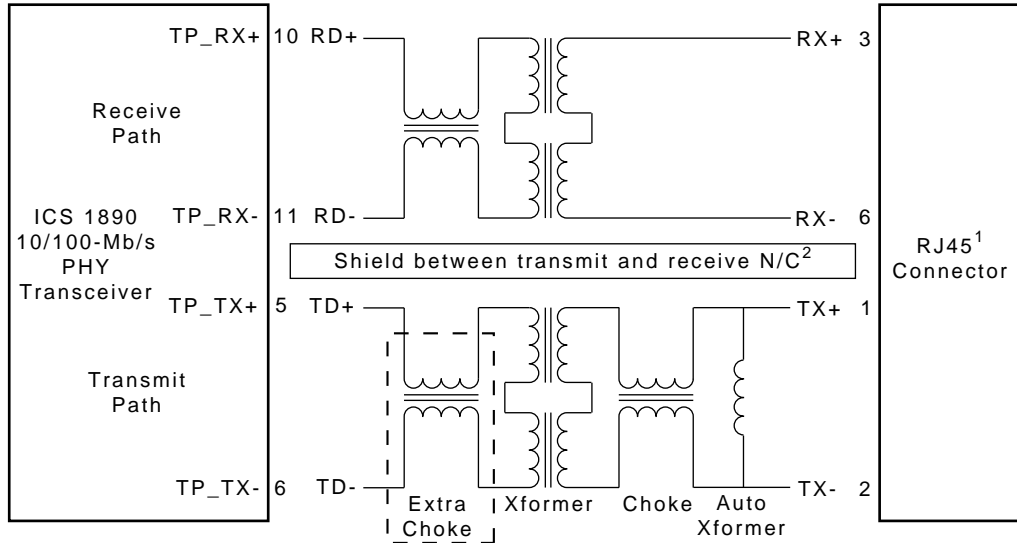
Table 17 10/100-Mb/s Magnetic Module Vendors

Manufacturer	No Choke Style Part Number	Extra Choke Style Part Number
Bel Fuse	—	S558-5999-01
Halo (singles)		
– With extra choke	TG32-3506ND	TG22-S010ND
– No choke	TG22-3506ND	—
– 3-wire choke (in place of autotransformer)	TG32-S020ND	—
Nano Pulse	NP16170-30	NP16120-30
Pulse Engineering	PE-68515	PE-68517
Valor	ST6118 ST6116	SF6035
Nano Pulse (SIP package)	—	NP16120-00

Figure 16 shows the data paths for the 10/100-Mb/s magnetics module.

ICS1890 Schematic Diagram Description

Figure 16 10/100-Mb/s Magnetics Module Data Paths

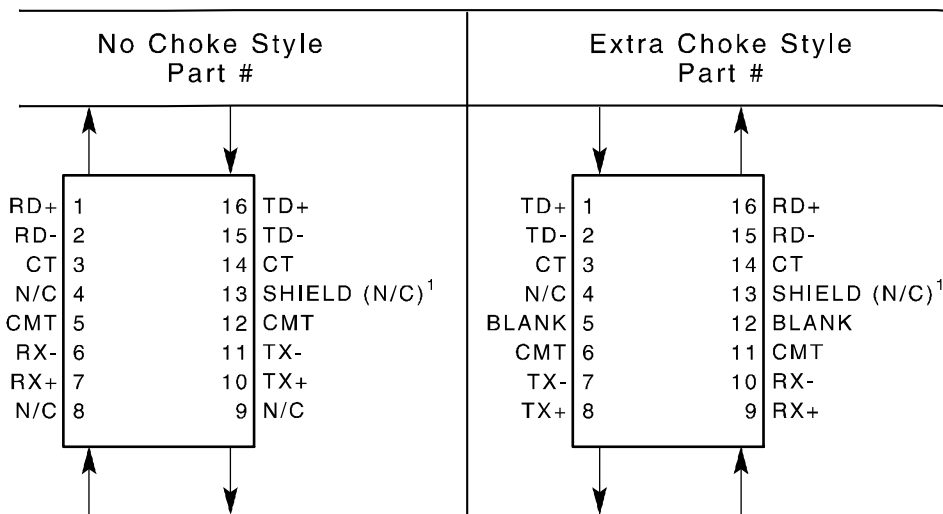


- ¹ The RJ45 pinout shown is for the NIC side of the link. The hub side typically implements crossover function by swapping the 3 and 6 and 1 and 2 pairs.
- ² The shield between transmit and receive is an option that is available from some vendors like Nano Pulse. A 0 Ω resistor connection from this pin to the shield ground should be used so that this pin can be left not connected (N/C) when using modules that do not support a shield.

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Figure 17 shows the footprints for both the no choke style and extra choke style transformers.

Figure 17 No Choke, Extra Choke Style Transformer Footprints



- ¹ The shield between transmit and receive is an option that is available from some vendors like Nano Pulse. A 0 Ω resistor connection from this pin to the shield ground should be used so that this pin can be left not connected (N/C) when using modules that do not support a shield.

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3.3.5 MII Data Interface

The MII data interface is a specification of signals and protocols that formalizes the interface of a 10/100-Mb/s Ethernet MAC to the underlying physical layer. This specification supports 100BASE-TX, 100BASE-T4, and 100BASE-FX physical type media transparently to the MAC. Table 18 maps the 21143 MII interface to the ICS1890 MII interface.

Table 18 21143 to ICS1890 Interface Signal Mapping

Signal	21143	Pin	ICS1890	Pin
Transmit clock	mii/sym_tclk	124	TXCLK	43
Transmit enable	mii_txen/sym_txd<4>	123	TXEN¹	44
Transmit error	—	—	TXER¹	42
Transmit data 3	mii/sym_txd<3>	119	TXD3	48
Transmit data 2	mii/sym_txd<2>	120	TXD2	47
Transmit data 1	mii/sym_txd<1>	121	TXD1	46
Transmit data 0	mii/sym_txd<0>	122	TXD0	45
Receive clock	mii/sym_rclk	128	RXCLK	37
Data valid	mii_dv	129	RXDV	36
Receive error	mii_rx_err/sel10_100	127	RXER	38
Receive data 3	mii/sym_rxd<3>	133	RXD3	32
Receive data 2	mii/sym_rxd<2>	132	RXD2	33
Receive data 1	mii/sym_rxd<1>	131	RXD1	34
Receive data 0	mii/sym_rxd<0>	130	RXD0	35
Carrier sense	mii_crs/sd	117	CRS	50
Collision detect	mii_clsn/sym_rxd<4>	118	COL	49
Management data clock	mii_mdc	134	MDC	31
Management data input/output	mii_mdio	135	MDIO	30

¹The 21143 does not support the transmit error function, so this pin should be grounded.

The MII data interface specifies both a 4-bit transmit path and a 4-bit receive path allowing for a transfer of a data nibble. The transmit path includes a transmit clock for synchronous transfers, a transmit enable signal, and a transmit error signal. The receive path includes a receive data clock for synchronous transfers, a receive data valid signal, and a receive error signal. The ICS1890 sources both the transmit clock and receive clock.

ICS1890 Schematic Diagram Description

3.3.5.1 Carrier Sense and Collision Detect Signals

Table 19 describes the operation of the MII Carrier Sense and Collision Detect signals.

Table 19 MII Carrier Sense and Collision Detect Signal Operation

In...	Carrier sense is...	Collision detect is...
Half-duplex mode	True when data is being transmitted or received.	True when data is being received while a transmission is in progress.
Full-duplex mode	True when data is being received.	Always false. Collisions never occur in this mode.

3.3.6 LED and PHY Pins

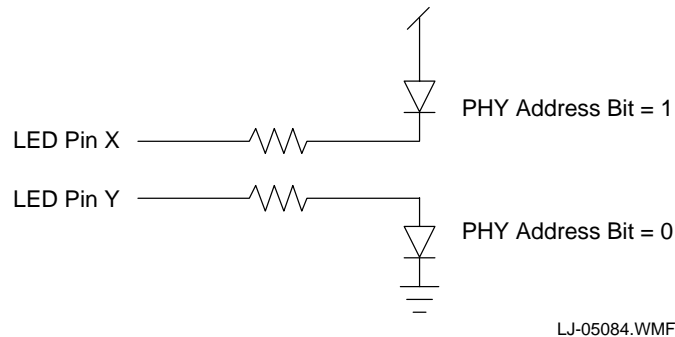
The ICS1890 device uses a unique pin-sharing scheme that allows the five LED pins to also be used to set the PHY address. During power-up and reset, these pins define the address of the PHY device. Following power-up and reset, these pins are used as status indicators.

The address of the PHY can be any number from 0 to 31. If an address of 0 is used for the PHY, the MII interface is isolated on power-up or reset and must be enabled through the MII management port (register 0, bit 10) as defined by the IEEE specification. All other address selections leave the MII interface active by default.

If both the 21143 and the ICS1890 are mounted directly on the same printed circuit board, an address of 1 for the PHY is recommended.

The actual value that is used for the individual address of the PHY depends on the configuration of the LED components (see Figure 18). When a value of “1” is needed, the LED and resistor are connected between the LED pin and **Vdd** (LED pin X). When a value of “0” is needed, the LED and resistor are connected between the LED pin and ground (LED pin Y). The special driver senses the polarity and adjusts its drive logic to appropriately turn the LED on or off. Resistor values should be in the range of 510 Ω to 10 k Ω (1/2 W). The recommended resistor value is 1 k Ω (1/2 W).

Figure 18 Configuring LED Components



If LEDs are not required for your application, only a resistor is required to set the address of the PHY. If LEDs are not required for your application and the ICS1890 will not be accessed by the serial MII management interface, only a single resistor to **Vdd**

on any one of the LED pins is required. This ensures that the address of the PHY is not 0, preventing the ICS1890 from being powered up in an isolated state without an enable from management to the MII interface.

3.3.7 ICS1890 Power Supply and Layout Considerations

It is very important to properly isolate the ICS1890 10/100-Mb/s PHY device from noise sources in a system design. The following are the two main areas of consideration for filtering noise:

- Isolation from 21143 noise
- Noise coupling between the ICS1890 transmitter and receiver

Two methods for isolating the 21143, transmit, and receive power supplies are described in Table 20.

Table 20 Methods for Filtering Noise

Method	Description
Using a single Vdd plane	Isolate the supply domains with ferrite beads and point-to-point routing as described in Table 21 and Figure 19. The corresponding ground pins are tied directly below to a single internal layer ground plane.
Using split Vdd planes	Connect the power pins to the planes directly below them (except for pin 56 which must be point-to-point trace routed as shown in Figure 20). As with the single Vdd method, all ground pins are tied directly below to a single ground plane.

Filtering for the ICS1890 is accomplished by separating the power supply into three domains: 21143, transmit, and receive. Table 21 lists all supply pins on the device into one of these three categories. Each supply pin is followed directly by its corresponding ground pin. Supply pins are shown paired up with their appropriate neighbor for bypass purposes. All ground pins are tied to a single ground plane below. Each supply pair should be bypassed with a 0.1 μ F capacitor located as close to the device as possible.

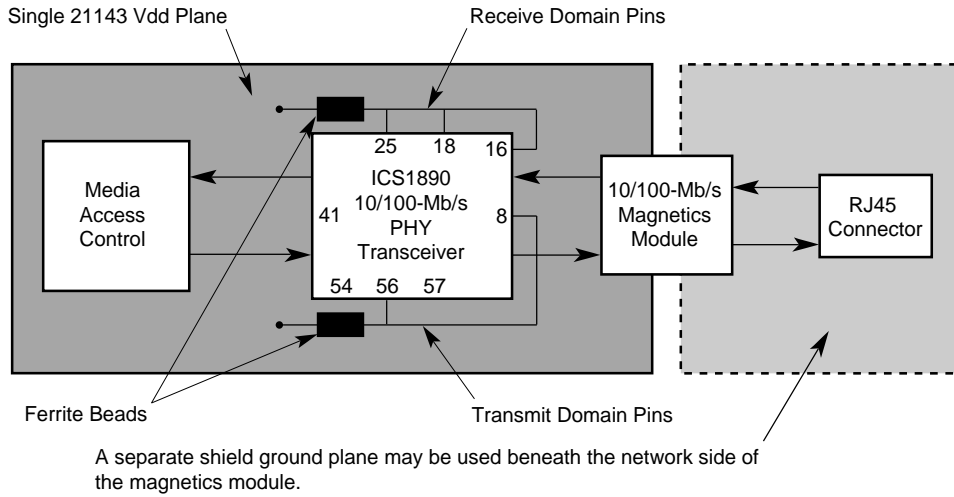
Table 21 Power Supply Filtering

21143 Domain	Transmit Domain	Receive Domain
41 Vdd	8 Vdd	16 Vdd
40 Vss	7 Vss	18 Vdd
		17 Vss
54 Vdd	56 Vdd	25 Vdd
51 Vss	55 Vss	29 Vss
57 Vdd	—	—
63 Vss		

Figure 19 illustrates a single **Vdd** plane isolation with point-to-point trace routing. The 21143 domain **Vdd** pins drop directly down to the single power plane while the transmit and receive domain pins are isolated using point-to-point routing and inline ferrite beads.

ICS1890 Schematic Diagram Description

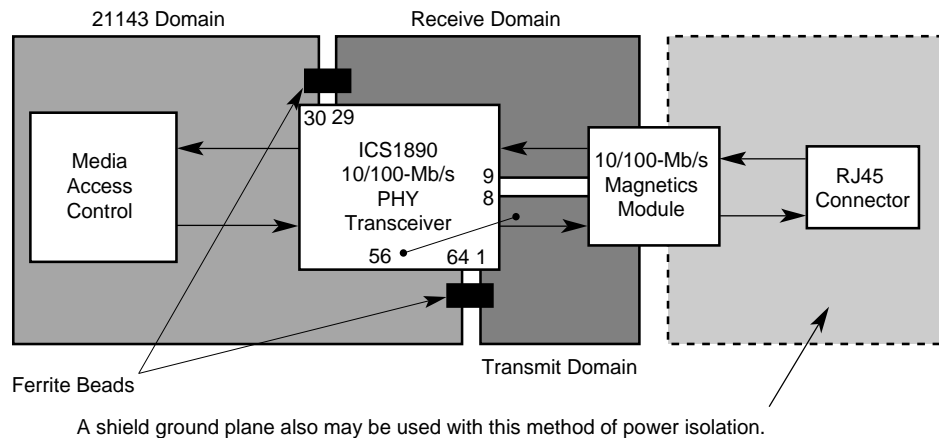
Figure 19 Single Vdd Plane Isolation



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Figure 20 illustrates split **Vdd** planes power supply isolation. The power planes must be split as shown in this figure. The pin number callouts specify where the power plane splits should occur in the board. Note that pin 56, transmit **Vdd**, is above the 21143 domain **Vdd** plane. This pin must be point-to-point trace routed to the transmit domain power plane as shown. All other power pins besides pin 56 connect directly to their corresponding power planes below them. A single, uniform plane should be used for ground. Both the receive and transmit domains should be connected to the 21143 domain through a ferrite bead or inductor.

Figure 20 ICS1890 Power Management Considerations



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3.3.7.1 Power Management Considerations

The ICS1890 supports the following two power saving modes:

- Low power —Activated by holding the **RESET** pin continuously low or by writing a logic one to the power-down bit (status register 0, bit 11). When the device is in low-power mode, all functions are disabled except for register access through the MII management interface. All register values are maintained during low-power mode, except for latching status bits that are reset to their default values.
- Automatic 100BASE-T power-down —Automatically reduces total power requirements when operating in 10BASE-T mode by powering down the 100BASE-TX modules.

Table 22 describes the power consumption values.

Table 22 ICS1890 Power Consumption

Power Consumption Value	Description
Total power consumption	Maximum power consumption is less than one watt and maximum supply current is 195 ma.
Low-power modes:	
<i>System reset mode</i>	Pin 22 held low causes ICS1890 to reset and enter low-power mode. Supply current is approximately 30 mA.
<i>Power-down mode</i>	Status register 0, bit 11, set to a logic 1 causes the ICS1890 to enter low-power mode with only management interface and logic remaining active. This action isolates the transmit data output and the MII. Supply current is approximately 10 mA.
<i>Reference input stop mode</i>	When the 25-MHz clock signal is removed (or stopped) the ICS1890 supply current drops to approximately 30 mA.
<i>Automatic 100BASE-TX power-down mode</i>	Extended control register 2 (register 19), setting bit 0 to a logic 1 with 10BASE-T selected for network connection, automatically turns off the 100BASE-TX transceiver. Automatic 100BASE-TX power-down mode supply current is approximately 100 mA.

Note : Power-down mode supply current values are not tested and are approximated. ICS advises its customers to obtain the latest version of all device data from ICS to verify that any information being relied on by the customer is current and accurate.

3.4 ICS1890 Summary

This section described how to design a 10/100-Mb/s adapter card using the 21143 and the ICS1890. Compatible vendor magnetic modules that use the no choke style and extra choke style were also listed. Layout considerations for filtering noise and isolating the 21143, transmit, and receive power supplies were also provided.

4 DP83840A MII PHY Network Implementation

This section contains the design recommendations for the National Semiconductor DP83840A 10/100-Mb/s PHY device and the DP83223V TWISTER High-Speed Networking Transceiver (referred to as the DP83840A and DP83223V) in a node application using the 21143.

4.1 DP83840A and DP83223V Overview

The DP83840A PHY device incorporates an integrated 10BASE-T transceiver as well as an MII for a connection to the 21143. The DP83840A is fully compatible with the DP83223V to enable 100BASE-TX compliant signaling.

A design based on these three devices allows for a simple low-cost PCI node design, which will support both 10BASE-T and 100BASE-TX protocols. The comprehensive feature sets of both the 21143 and the DP83840A support several different modes of functionality.

Although design issues such as common magnetics, autonegotiation, and 10/100-Mb/s operation are noted here, detailed emphasis is placed on fundamental design requirements from the MAC layer to the RJ45-8 connector. Schematic diagrams, layout considerations, and power requirements are all provided in this application note. A magnetics scheme is recommended to help the designer integrate the National Semiconductor parts in a system.

For a given application, the component values and design suggestions in this section can and will vary with the particular design. This section illustrates the function of the various components and their relationship to overall system performance. With this knowledge, the system designer can make modifications to the recommendations with an understanding of the potential impact to the system.

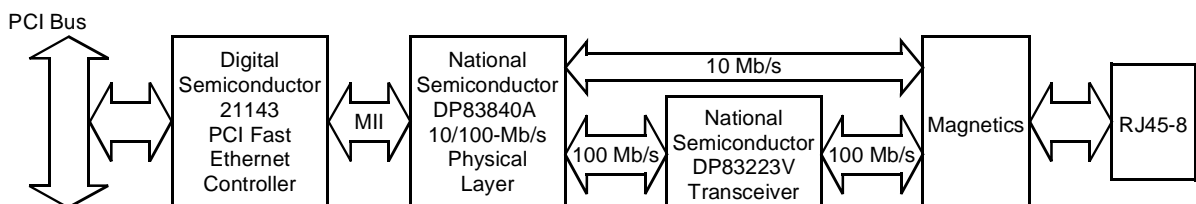
This section should be reviewed in conjunction with all documentation available on the products covered in this application note from both Digital Semiconductor and National Semiconductor. (See Appendix B.)

See Appendix B to order data sheets and product samples of the DP83840A PHY device and the DP83223V transceiver.

4.2 DP83840A and DP83223V Block Diagram

Figure 21 is the system diagram for a node application. The following sections describe the blocks. For more detailed information on the specifications of these parts, see the documentation listed in Appendix B.

Figure 21 10/100-Mb/s Block Diagram



4.3 DP83840A Description

The DP83840A finds wide application in data communication systems. It is a PHY device for Ethernet 10BASE-T and 100BASE-X using Category 5 (CAT5) unshielded, Type 1 shielded, and fiber-optic cables. It interfaces to the PMD sublayer through a DP83223V and to the MAC layer through the MII, ensuring interoperability between products from different vendors.

The DP83840A system architecture is based on the integration of the following National Semiconductor industry-proven core technologies:

- 10BASE-T ENDEC/Transceiver module to provide the 10-Mb/s IEEE 802.3 functions
- 100BASE-X physical coding sublayer (PCS) and control logic that integrate the core modules into a dual-speed Ethernet physical layer controller

The DP83840A features include:

- IEEE 802.3 10BASE-T compatibility. ENDEC and UTP/STP transceivers and filters are built in.
- IEEE 802.3 100BASE-X compatibility with support for Category 5 UTP, Type 1 STP, and fiber-optic transceivers. Connects directly to the DP83223V.
- ANSI X3T12 TP-PMD compatibility.
- IEEE 802.3 autonegotiation for automatic speed selection.
- Independent interface (MII) with serial management interface.
- Integrated, high-performance, 100-Mb/s clock recovery circuitry that requires no external filters.
- Full-duplex support for 10 Mb/s and 100 Mb/s.
- MII serial 10-Mb/s output mode.
- Programmable loopback modes for easy system diagnostics.
- Flexible LED support.

4.4 DP83223V Description

The DP83223V twisted-pair transceiver can drive and receive either binary or MLT-3 encoded data streams. The DP83223V allows links of up to 100 m (328 ft) over both STP and data grade UTP or equivalent. The DP83223V also provides important features such as tristate-capable transmit outputs, and controlled transmit output edge rates (to reduce EMI radiation) for both binary and MLT-3 modes of operation.

The DP83223V features include:

- Integrated transmitter and receiver with adaptive equalization circuit.
- Programmable binary or MLT-3 operation.
- Isolated TX and RX power supplies for minimum noise coupling.
- Controlled transmit output edge rates for reduced EMI.
- Tristate-capable current transmit outputs.
- Loopback feature for board diagnostics.
- Programmable transmit voltage amplitude.

In addition to the above features, the DP83223AV implements an integrated baseline restoration circuit.

4.4.1 Magnetics

The magnetics block in Figure 21 uses a common magnetics scheme that allows 10-Mb/s and 100-Mb/s data to coexist in the same magnetics package. The concept of common magnetics is based on the interoperation of the DP83840A and the DP83223V, and allows for either 10-Mb/s or 100-Mb/s operation with the use of a single magnetics module and RJ45-8 media connector. (For a complete discussion of the common magnetics concept, refer to the National Semiconductor *10/100 Ethernet Common Magnetics* application note.)

National Semiconductor has patents on a common magnetics scheme, and provides a license to purchasers of both the DP83840A and the DP83223V components to use the common magnetics scheme in their design. Several suppliers have indicated that they intend to provide magnetic components for the National Semiconductor recommended implementation. Appendix A contains a list of these magnetics vendors and the license agreement. This is not an exhaustive list and other vendors could be considered, but the transformer would need to be characterized in relation to the *10/100 Base-T Magnetics Specification* (available from National Semiconductor).

4.4.2 DP83840A and DP83223V Schematic Diagram

Appendix A contains the schematic diagrams for the PHY. Figure 40 illustrates the interconnection of the DP83840A and DP83223V.

4.4.3 Media-Independent Interface (MII)

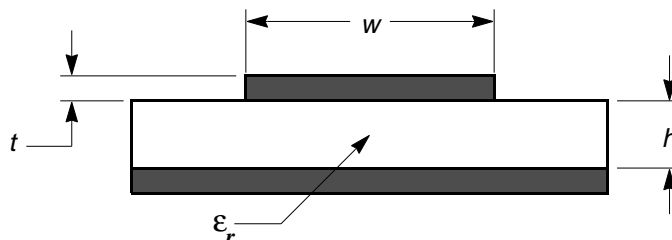
The DP83840A has a standard IEEE 802.3 MII for connection to external 10-Mb/s or 100-Mb/s PHYs. This comprises nibblewide (4-bits) transmit and receive data streams, transmit and receive clocks, transmit enable, receive collision, receive carrier sense, receive data valid, data error, and serial management data clock and data signals. These signals are: **TX_CLK**, **TXD[3:0]**, **TX_EN**, **CRS**, **COL**, **RXD[3:0]**, **RX_CLK**, **RX_DV**, **RX_ER**, **MDC**, and **MDIO**.

The MII supports two nibble clock rates: 2.5 MHz for 10-Mb/s operation and 25 MHz for 100-Mb/s operation. Operation at 10 Mb/s or 100 Mb/s is transparent to the host.

4.4.4 Signal Terminations

The trace impedance of each MII line should be approximately 68Ω per the IEEE specification. The design of microstrips for PC boards is straightforward and a function of the microstrip width (w), thickness (t), height (h), and the relative electric permittivity of the substrate (ϵ_r), as shown in Figure 22.

Figure 22 Microstrip impedance



Equation 1 shows how the various geometric and material parameters on the printed circuit board (PCB) control the impedance of the trace. Most of the PCB programs calculate the trace impedance directly.

Equation 1 Microstrip Impedance

$$Z = \left(\frac{87}{(\sqrt{\epsilon_r} + 1.41)} \right) \ln \left(\frac{5.98h}{(0.8w + t)} \right)$$

The DP83840A supports 10-Mb/s and 100-Mb/s Ethernet using the DP83223V and the common magnetics approach. The following signal lines between the DP83840A and the DP83223V should be PECL (Thevenin) terminated at the DP83223V: **PMRD+**, **PMRD-**, **PMID+**, **PMID-**, **SD+**, and **SD-**. These signal lines are Thevenin terminated (see Figure 42) with an equivalent resistance equal to the trace impedance. This trace impedance should be controlled and match the device termination resistance. For the preferred case of a 50-Ω transmission interconnect, resistors R23 through R28 are 82.5 Ω to **Vcc**, and R6 through R9, R21, and R22 are 130 Ω to ground. This generates a 50.3-Ω Thevenin resistance. The trace impedance of these signal lines should also be 50 Ω.

It is critical that these lines be kept short (<1 inch) and that the termination resistors are as close as possible to the destination. If the PECL termination resistors are not placed close to the signal destination, reflections might result and could corrupt the signal integrity. The midlevel voltage of the termination network should be 3.0 V and the required bias current is 23.5 mA due to each line termination.

The 50-Ω termination is the low impedance robust approach, requiring 23.5 mA per PECL termination. In this application there are six terminations totaling 141 mA. This might be excessive current draw for certain applications and higher values of termination resistance could be considered. For example, in the National Semiconductor *Unmanaged Repeater* application note, the termination values are 160 Ω to **Vcc** and 260 Ω to ground. This is a 100-Ω Thevenin resistance and the current draw is reduced to 11.75 mA per termination. A reasonable upper bound might be a Thevenin resistance of approximately 100 Ω to 200 Ω. To ensure that the data maintains integrity as the resistor values increase, check the quality of the high-speed interconnect signal with an oscilloscope, looking for minimal ringing and equal rise and fall times in the waveform.

In Fast Ethernet systems, special attention needs to be given to transmission type effects. If proper line termination is not used for a given application, ringing will occur on these lines. It is worth noting that the **SD±** signal detect lines are detecting either the presence of a valid signal on the **RXI±** inputs or that loopback mode has been selected. In either case, **SD±** is essentially static and higher value termination resistors can be used.

4.4.4.1 Signal Transmission

When the 100-Mb/s port is enabled, the DP83223V **TXO±** outputs are directly connected across the entire primary of the common magnetics transmit section of the transformer. Because this connection uses a 1:1 isolation transformer, the 2-V peak-to-peak (5%), differential MLT-3 signal generated by the DP83223V is maintained as it is coupled onto the UTP. The 100-Mb/s operation uses the transmit transformer in a unity-gain configuration (less the insertion loss). The source termination resistance is established by the sum of R4 and R5 (47.5 Ω × 2.5), and the ON resistance of the

solid-state switches Q3 and Q4 ($2.5 \Omega \times 2$), as shown in Figure 43. This circuit resistance should be equal to the cable impedance of 100Ω . For STP, the circuit resistance of R4, R5, Q2, and Q3 should be equal to the cable impedance of 150Ω .

The DP83840A **TXU** \pm output provides standard 10BASE-T signaling, as shown in Figures 41 and 42 in Appendix A, and Figure 2 of the National Semiconductor *10/100 Ethernet Common Magnetics* application note. This differential signal is coupled to one-half of the transmit isolation transformer primary winding through series resistors R1 and R2, and capacitors C32 and C30. Equation 2 shows the basic transformer equations.

Equation 2 Transformer Equations

$$\text{A. } \frac{V_p}{V_s} = \frac{n_p}{n_s} = N$$

$$\text{B. } Z_{prim} = N^2 Z_{sec}$$

Equation 2A is the turns ratio as a function of the secondary and primary voltages, and Equation 2B is the primary impedance as a function of the secondary load and turns ratio (N). In Equation 2, subscripts *p* and *s* represent primary and secondary, *V* represents voltage, and *Z* represents impedance.

In 10BASE-T transmit mode, the turns ratio (n_p/n_s) is 1/2. The secondary load impedance for UTP cable is 100Ω . For the primary impedance to match the secondary impedance, a primary impedance of 25Ω is required. This scales through the transformer voltage gain to appear as 100Ω . This primary impedance is established by resistors R1 and R2 (10.5Ω each) and the output impedance of the driver ports **TXU** \pm (2.5Ω each) (see Figure 42). The series sum of these resistances is 25Ω .

Good signal transfer is maintained by matching the cable impedance to the driving impedance. Resistor R3 and capacitors C1 and C8 are included to provide a balanced impedance across each leg of the transmit transformer primary winding and high-frequency rolloff, which improves FCC characteristics.

Bypass capacitors C29 to C32 and C8 have been added since the initial work on the 10/100 common magnetics. These capacitors compensate for the rising output impedance of the 10-Mb/s transmit driver circuits. This circuit establishes a pole-zero pair, with the zero being at approximately 15 MHz. Placing the zero at 15 MHz balances the increasing output impedance term. The effect of adding these capacitors is a 2-dB to 3-dB improvement in transmit return loss measurement. These capacitors, which increase the output transmit voltage, should be added to existing and new designs if possible.

4.4.4.2 Signal Receive Operation

As shown in Figure 40 in Appendix A and Figure 3 of the National Semiconductor *10/100 Ethernet Common Magnetics* application note, the 100-Mb/s receive signal is coupled from the cable by an isolation transformer with a 1:1 turns ratio. The DP83223V **RXI** \pm inputs receive the 100-Mb/s data through the attenuation network comprising resistors R29 through R32 and capacitor C14. This attenuation network is required to optimize the adaptive equalization function within the DP83223V receiver.

A recent application note from National Semiconductor, *DP83223 TWISTER Adaptive Equalization Considerations*, discusses the attenuation network details and component selection.

A particular system design must take into account the actual amount of transformer insertion loss. This measured value of insertion loss and the manufacturer-specified tolerances can be used to determine the correct resistor divider ratio for the network attenuator. It is critical that the overall attenuation resistance be maintained at 100 Ω (series resistance of R29 through R32). The attenuation circuit (shown in Figure 42) comprises two series 12.1- Ω resistors (R31 and R32), which provide a 24.2- Ω differential impedance to the incoming signal. Additionally, R29 and R30 form a 76- Ω combination that, when combined with the 24.2- Ω series resistance, creates the required 100- Ω forward cable termination. The attenuation network resistors should have a tolerance of $\leq 1\%$ (1/8 Watts) to maintain signal tolerance. The DP83223V **RXI \pm** inputs receive the signal as it appears across the attenuator voltage divider. This attenuated voltage should be 1.45 V. Measurements should be made on the system to ensure that the correct voltage is being received. This method of measurement is described in the *DP83223 TWISTER Adaptive Equalization Considerations* application note from National Semiconductor.

Capacitor C14 (0.01 μ F) is placed at the center point of the attenuation resistors. This capacitor provides common-mode ground reference, reducing system sensitivity to common-mode noise.

Note: The selection of the attenuation network components is extremely critical for good system performance. Refer to the *DP83223 TWISTER Adaptive Equalization Considerations* application note from National Semiconductor for the detailed design of this circuit.

An isolation transformer with a 1:1 turns ratio couples the 10-Mb/s differential receive signal from the cable. This differential signal is capacitively coupled through C9 and C10 to the DP83840A **RXI \pm** inputs (see Figure 41). Because the signals are capacitively coupled to the DP83840A **RXI \pm** high-impedance inputs, dc current is blocked, ensuring signal levels with the proper common-mode voltage as set by the DP83840A. In addition to the Manchester encoded 10BASE-T data, the DP83840A **RXI \pm** inputs receive normal link pulses and fast link pulses to allow Nway autonegotiation functionality.

4.4.5 STP Operation

The DP83840A can be configured, through internal control register access, to source data through the **TXS \pm** outputs for shielded twisted-pair operation. In this case, the unshielded **TXU \pm** outputs are tristated to eliminate contention. Similarly, the **TXS \pm** outputs are tristated during 10-Mb/s unshielded twisted-pair signaling from **TXU \pm** .

Other than resistor and capacitor value changes to accommodate 150- Ω STP cable, all remaining interaction between the DP83840A and the DP83223V remains as stated in Sections 4.4.3 through 4.4.5. Additionally, the RJ45-8 modular jack used for

DP83223V Description

unshielded twisted-pair applications is replaced by a media connector (DB-9). Refer to Section 4.4.7 for the connection information. Table 23 lists the component values required for STP or UTP operation.

Table 23 Component Values Required for STP or UTP Operation

Configuration	R3	C8 (pF)	C1 (pF)	R10	R4	R5	R16 R17	R1 R2	C29/C31 (pF)	C30/C32 (pF)	R31 R32	R29 R30
UTP	10.5	1000	9	511	47.5	47.5	×	10.5	×	1000	12.1	37.9
STP	16.5	620	18	511	73.2	73.2	16.5	×	620	×	29.4	46.4

× = Do not install component.

4.4.6 Common-Mode Termination

The intent of common-mode termination is to help reduce unwanted contributions to EMI emissions and susceptibility by properly terminating the common-mode energy that can exist on the twisted-pair cable. This technique is designed for unshielded twisted-pair applications that, due to the lack of a shield, inherently possess high susceptibility to common-mode noise sources.

4.4.6.1 Transmit Active Pair Termination

Figure 43 and the *10/100 Base-T Common Magnetics* specification suggest the use of a center-tapped transformer within the transmit magnetics. This allows access to the common-mode signal present on the cable. The impedance of the common-mode channel within an unshielded twisted-pair can be calculated to be approximately 75 Ω. To obtain the 75-Ω common-mode resistance, R18 (49.9 Ω) is connected between the transformer center-tap and capacitor C5 (500 pF to 1000 pF @ 2 kV rms). This resistance, when combined with the cable differential termination resistance, provides the required 75-Ω resistance. The other side of C5 is connected to chassis ground. This capacitor requires a 2-kV rms rating to guard against high-energy transients coupled onto the LAN cable systems and static-charge buildup on LAN cables and components. The *TP-PMD* specification (Sections 8.4 to 8.4.2.2, Isolation Requirements) establishes the voltage rating for the capacitor. The inclusion of this capacitor also improves circuit performance, providing a solid common-mode reference and reducing common-mode noise.

The high voltage capacitor can be fabricated using the printed circuit board as the dielectric. The capacitor should be designed onto the chassis side of the board, using all four layers to obtain the required capacitance. Equation 3 is the equation for a parallel plate capacitor.

Equation 3 Parallel Plate Capacitance

$$C = 8.85 \left(\frac{\epsilon_r A}{l} \right)$$

In Equation 3, C is in F, A is the area of the plates in m², l is the separation of the plates in m, and ε_r is the relative permittivity of the medium between the capacitor plates, in Fm⁻¹.

Dielectric strength (DS) is a critical parameter of this capacitor. This is the voltage that can be placed across the part prior to breakdown. For a given plate spacing this breakdown is proportional to the dielectric strength of the medium between the plates. The radius of curvature of the edge of the capacitor plate is another factor. With the printed circuit board as the medium (which is essentially epoxy/fiberglass), the DS is 400 V/mil. For a standard 4-layer board with an overall thickness of 0.062 in, the dielectric strength is approximately 6400 V between capacitor plates.

4.4.6.2 Receive Active Pair Termination

Figure 43 shows R57 (49.9 Ω) connected to the center-tap of the receive transformer primary to provide a common-mode attenuation connection point.

4.4.6.3 Unused Pair Termination

Unused pairs 4-5 and 7-8 are tied together and connected to the same 2-kV rms capacitor (C5) through two 75-Ω resistors (R19 and R20). This provides direct termination for potential common-mode noise on the unused pairs. Because of cross-talk, common-mode noise present on the unused pairs can also be detrimental.

4.4.7 Media Connections

Tables 24 and 25 show the pinout requirements for UTP and STP node connections.

Table 24 Unshielded Twisted-Pair RJ45-8 Connector

10BASE-T/100BASE-TX	Pin
Transmit pair	1 (TX+) and 2 (TX-)
Receive pair	3 (RX+) and 6 (RX-)
Unused pair	4 and 5
Unused pair	7 and 8

Table 25 Shielded Twisted-Pair DB-9 Connector

10BASE-T/100BASE-TX	Pin
Transmit pair	5 (TX+) and 9 (TX-)
Receive pair	1 (RX+) and 6 (RX-)
Unused pins	2, 3, 4, 7, and 8
Ground to chassis	Shield

4.5 DP83840A and DP83223V Layout Considerations

The goal of any complex system design, especially one that includes both analog and digital functionality, is to achieve the most robust system performance possible. Performance aspects such as bit error rate, EMI, and general signal integrity must be considered.

The correct combination of component placement, signal routing practices, and power supply distribution will yield a robust and reliable system.

DP83840A and DP83223V Layout Considerations

This section considers the physical design aspects of a 10/100 Ethernet system design using National Semiconductor PHYs in conjunction with common magnetics. The National Semiconductor *1996 National Ethernet Databook* discusses the theory and practice of system design.

4.5.1 Component Placement

The relative placement of the active and passive components within a system design is essentially defined by important design parameters; such as performance, cost, and board area.

Figure 23 shows a potential component layout that will yield good signal integrity and good overall performance. The layout minimizes the required board area while optimizing the relative component placement.

The layout of the dynamic transmit and receive signals at the twisted-pair transceiver interface is critical to good performance. As shown in Figure 23, the DP83840A is oriented such that its **TD**, **RD**, and **SD** signal pins are in close proximity to the **PMRD**, **SD**, and **PMID** signals on the DP83223V. These signals carry the transmit and receive 100-Mb/s data and their length should be minimal. This configuration shows the MII connector adjacent to the DP83840A pins that contain the MII signals (pins 51-80). The oscillator is adjacent to the **OSC_IN** pin on the DP83840A. Keeping the oscillator close to the device minimizes jitter at the clock output. Clearly, component location can vary depending on the other devices being used in the application.

Note: In the system layout it is critical to maintain short distances between the transmit and receive sections of the DP83840A and DP83223V, and to place the MII adjacent to the DP83840A (pins 51-80).

4.5.1.1 Special Considerations

Incorporate controlled impedance routing for the signal traces that carry the 125-Mb/s serial bit stream. Standard microstrip or stripline techniques are recommended. Choose an impedance of 50 Ω for each trace that transports the 125-Mb/s information between the RJ45-8, common magnetics, and the DP83223V transceiver. This is required to match the 100- Ω differential impedance of the unshielded twisted-pair cable.

The 125-Mb/s PECL signals connected between the DP83223V and the DP83840A can be designed as 50- Ω to 100- Ω impedance traces. The choice of PECL terminating resistors will determine the trace impedance, such that they are consistent with each other.

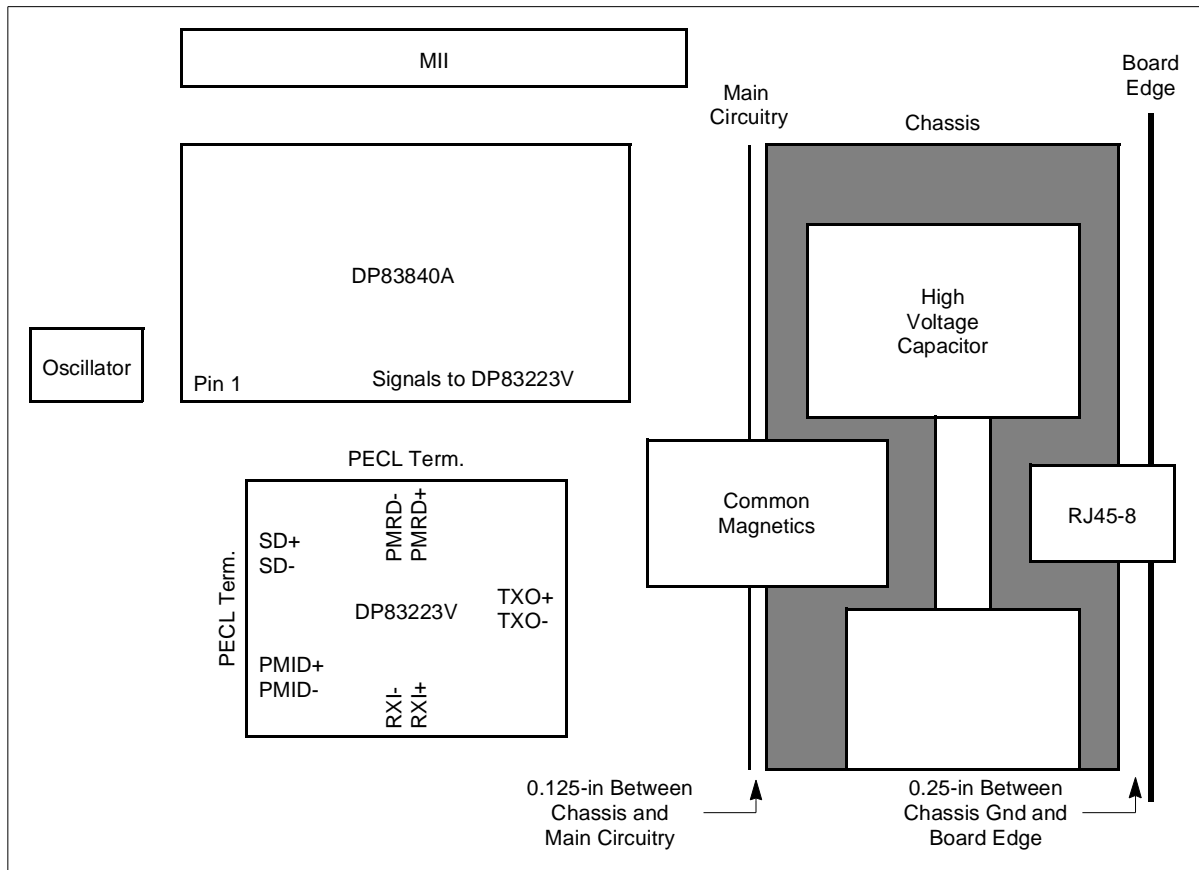
4.5.2 General Guidelines

General guidelines for optimal signal trace routing practices include:

- Minimal length, controlled impedance signal traces to minimize reflections and decrease noise sensitivities. The most critical signals are between the DP83840A and the DP83223V, and the signals from the RJ45-8 to the transformer. The signal traces from the RJ45-8 to the transformer should be stripline with an impedance of 50 Ω .
- Matched length differential signal traces to minimize jitter.
- Radiused, route trace corners of $>45^\circ$.

- Minimum number of vias for a given signal trace to minimize radiation.
- PECL terminations placed close to signal destination.
- All controlled impedance signal traces routed directly over or under uninterrupted power or ground planes on adjacent layers. This minimizes noise coupled into signal lines.

Figure 23 Physical Layer Component Placement Recommendation



4.5.3 Board Layers

The number of board layers will vary depending on the signal routing density. In general, a 4- to 6-layer design is sufficient. The 4-layer case shown in Figure 24 is sufficient for most node applications.

Figure 24 shows one potential option for PCB layer assignment, a configuration with good FCC results. Layers 1 and 4 are for signal routing, layer 2 is the ground plane, and layer 3 is V_{CC} for the circuit devices. On the chassis side of the card, layer 1 is chassis ground, layer 2 is for signals and capacitor, layer 3 is chassis ground, and layer 4 is the capacitor plate. For the capacitor, layer 2 is connected to 4 (as one plate) and layers 1 and 3 are the ground side of the capacitor. Configuring the capacitor in this way has the net effect of three capacitors in parallel.

Power Requirements

Figure 24 Board Layer Recommendation

	Main Circuitry	Chassis Side
1	Signal routing	Chassis ground
2	Ground plane	Signals and capacitor
3	Vcc	Chassis ground
4	Signal routing	Capacitor plate

4.5.4 Ground Plane Partitioning

Recent system measurements at National Semiconductor show that the single ground-plane approach is one way to minimize EMI. Ground-plane partitioning can cause increased EMI emissions that might make the system noncompliant with specific FCC regulations. Figure 23 shows a recommended ground layout scheme and specifies the placement and space between the system ground and chassis ground.

Keeping the chassis ground approximately 0.25-inches from the edge of the system motherboard, and voiding that gap of any copper, will help to reduce any potential fringe radiation that might occur during system operation. This is permissible because no active traces need to be routed in this area.

4.6 Power Requirements

Careful power supply filtering and isolation practices can provide a minimized noise environment for each of the unique digital and analog sections of the DP83223V and DP83840A. A recommendation is to use one power and one ground plane. Recent system measurements made at National Semiconductor on a 10/100 Ethernet system showed reduced (approximately 7 dB) EMI emissions in single ground and **Vcc** plane systems (as compared to multiple **Vcc** and ground islands interconnected by ferrite beads).

As the data rates begin to increase, power and ground-plane partitioning require careful consideration. To be compliant with electrical isolation issues, the chassis ground needs to be physically isolated from the system circuit ground. The dc voltage for the circuit card should be derived from a stable power supply. The power supply input decoupling circuit should provide sufficient capacitance that will maintain the supply at a full voltage and provide a low impedance at high frequencies. Typically, a capacitor to keep the voltage stable (10 μ F or 4.7 μ F) and a high-frequency bypass capacitor (0.01 μ F) are sufficient for the card if the supply is stable and clean. Careful attention to power decoupling is required on the PHYs and is described in Section 4.6.1.

4.6.1 DP83840A and DP83223V Decoupling

The DP83840A internally partitions the power sections into four basic groups: PLL, analog (ANA), RX/TX, and digital. To maintain the integrity of these power partitions, PLL, RX/TX, ANA, and digital power pins are decoupled as shown in Figure 41. The schematic shows a typical connection with parallel 10- μ F and 0.01- μ F capacitors, and a series inductor (C24, C4, and L3 [Murata BLM31A02]) to the **Vcc** power plane. This allows for the attenuation of low- and high-frequency noise. For the PLL and ANA **Vcc**, a series resistor can be added to provide further isolation. The value of this resistor should be $< 4 \Omega$ to keep the voltage drop low.

In certain applications it might be possible to simplify the decoupling circuit on these pins. The best way to determine if this is the case, is to measure the power supply noise using a spectrum analyzer on the power input and at the device pin. If this value is not influenced by the decoupling circuit, it might be possible to simplify the circuit. The present scheme provides good isolation, filtering, and voltage stability. For local decoupling on the DP83223V, connect RX and TX together with a large pad, and use 10- μ F and 0.01- μ F capacitors in parallel and a series inductor to the power plane. Figures 41 and 42 show the details of chip decoupling.

4.7 DP83840A and DP83223V Parts List

Table 26 lists the recommended parts for the DP83840A and DP83223V. .

Table 26 Recommended Parts List for DP83840A and DP83223V (Sheet 1 of 2)

Description	Value	Volts	Tolerance	Package	Qty	Reference
C/CER	9 pF	50	10%	SMD0805	1	C1
C/CER	27 pF	50	10%	SMD0805	1	C35
C/CER	620 pF	50	10%	SMD0805	2	C29, C31
C/CER	1000 pF	50	20%	SMD1206	2	C30, C32
C/CER	0.01 μ F	50	20%	SMD1206	14	C2, C6, C11-C18, C22-C25
C/CER	820 pF	50	10%	SMD1206	1	C8
C/CER	0.1 μ F	50	20%	SMD1206	2	C9, C10
C/CER	500 - 1000 pF	2 kV rms	20%	Through-hole	1	C5
Polarized capacitor	10 μ F	16	20%	SMD	9	C3, C4, C7, C19-C21, C26, C28, C36
Inductor	—	—	—	SMT	3	L1- L3
Telco connector	—	—	—	TH	1	J2
MII 100-Mb/s connector	—	—	—	RT/A_PCB_CONN	1	J1
Oscillator 50 MHz	—	—	—	Half-size	1	Y3
LED	Green	—	—	LED-dial 5-50 typ05	5	D2-D6
Resistor	1.5 k Ω	—	5%	r500	1	R63
Resistor	10.5 Ω	—	1%	1206	1	R3
Resistor	16.5 Ω	—	1%	1206	2	R16, R17
Resistor	10 k Ω	—	5%	1206	1	R59
Resistor	75 Ω	—	5%	1206	2	R19, R20
Resistor	10 Ω	—	5%	0805	1	R56
Resistor	10 k Ω	—	5%	0805	7	R49, R51-55, R59

DP83840A and DP83223V Summary

Table 26 Recommended Parts List for DP83840A and DP83223V

(Sheet 2 of 2)

Description	Value	Volts	Tolerance	Package	Qty	Reference
Resistor	1.5 k Ω	—	5%	0805	9	R14, R15, R42, R43, R60-R63
Resistor	4.7 k Ω	—	5%	0805	8	R34-R40, R64
Resistor	12.1 Ω	—	<1%	0805	2	R31, R32
Resistor	10.5 Ω	—	1%	0805	2	R1, R2
Resistor	37.9 Ω	—	<1%	0805	2	R29, R30
Resistor	47.5 Ω	—	1%	0805	2	R4, R5
Resistor	82.5 Ω	—	1%	0805	6	R23-R28
Resistor	130 Ω	—	1%	0805	6	R6-R9, R1, R22
Resistor	511 Ω	—	1%	0805	1	R10
Resistor	TBD ¹	—	1%	0805	4	R12, R13
Transistor	—	—	—	sot23	3	Q1-Q3
DP83223V	—	—	—	28PLCC	1	U2
DP83840A	—	—	—	PQFP100	1	U1
Fuse	—	—	—	Radial	1	F1
10/100 magnetics	—	—	—	SMD	1	T1

¹Design-dependent value.

4.8 DP83840A and DP83223V Summary

National Semiconductor provides a complete physical solution for 10/100 Ethernet. The component values and design suggestions in this section might vary for a given application. This section described the function of the various components and how they relate to system performance. With this information the system designer can modify the recommendations with an understanding of the potential impact.

Note: This design recommendation is presently being investigated in the laboratory and through computer simulation. These results will be made available to National Semiconductor customers.

5 BCM5000 MII PHY Network Implementation

This section describes how to interface the 21143 with the Broadcom BCM5000 10/100BASE-T4 Fast- Φ (referred to as the BCM5000).

5.1 BCM5000 Overview

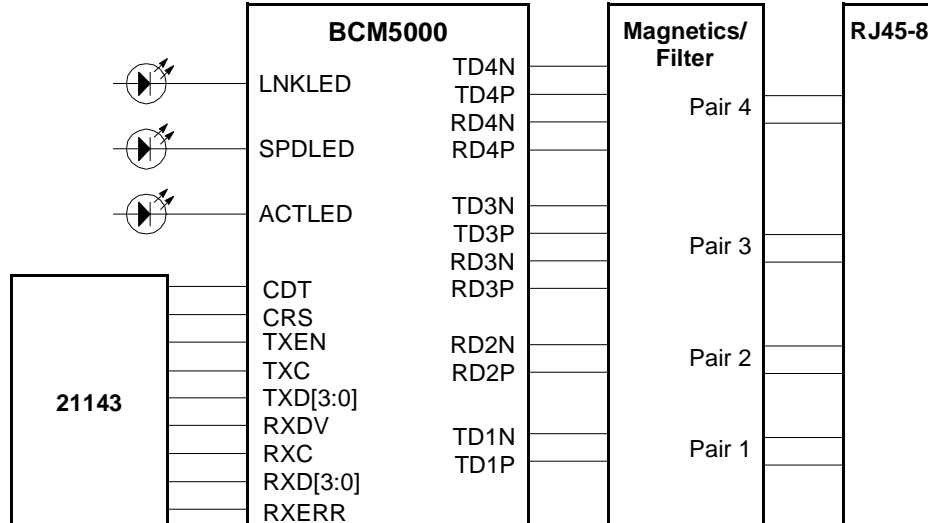
The BCM5000 is a single CMOS chip that performs all the physical layer interface functions for 100BASE-T4, 10BASE-T, and 10BASE-T full-duplex Ethernet on CAT3, 4, or 5 unshielded twisted-pair (UTP) cable. The BCM5000 is fully compliant with the IEEE 802.3 and the MII specification.

The chip receives and transmits data on UTP in the form of 8B6T for 100BASE-T4 and Manchester code for 10BASE-T. The BCM5000 connects directly to the T4 magnetics and recovers data and clock from the incoming signals. The recovered data stream is then decoded and output through the MII interface. For packet transmission, the binary data stream is received through the MII interface, encoded, and then transmitted through the interpolating line drivers out to the T4 magnetics.

5.2 BCM5000 Block Diagram

Figure 25 is a block diagram of an adapter based on the 21143 and the BCM5000.

Figure 25 Adapter Card Application



5.3 Using the BCM5000

This section provides schematic information and the requirements for using the BCM5000.

5.3.1 Schematics

Figure 26 shows how to connect the BCM5000 to the 21143.

5.3.2 Reset Requirements

The BCM5000 requires a hardware reset on power-up. Subsequent resets, if required, might be done in software through the MII management interface. The following suggestions are some possible ways to generate the hardware reset:

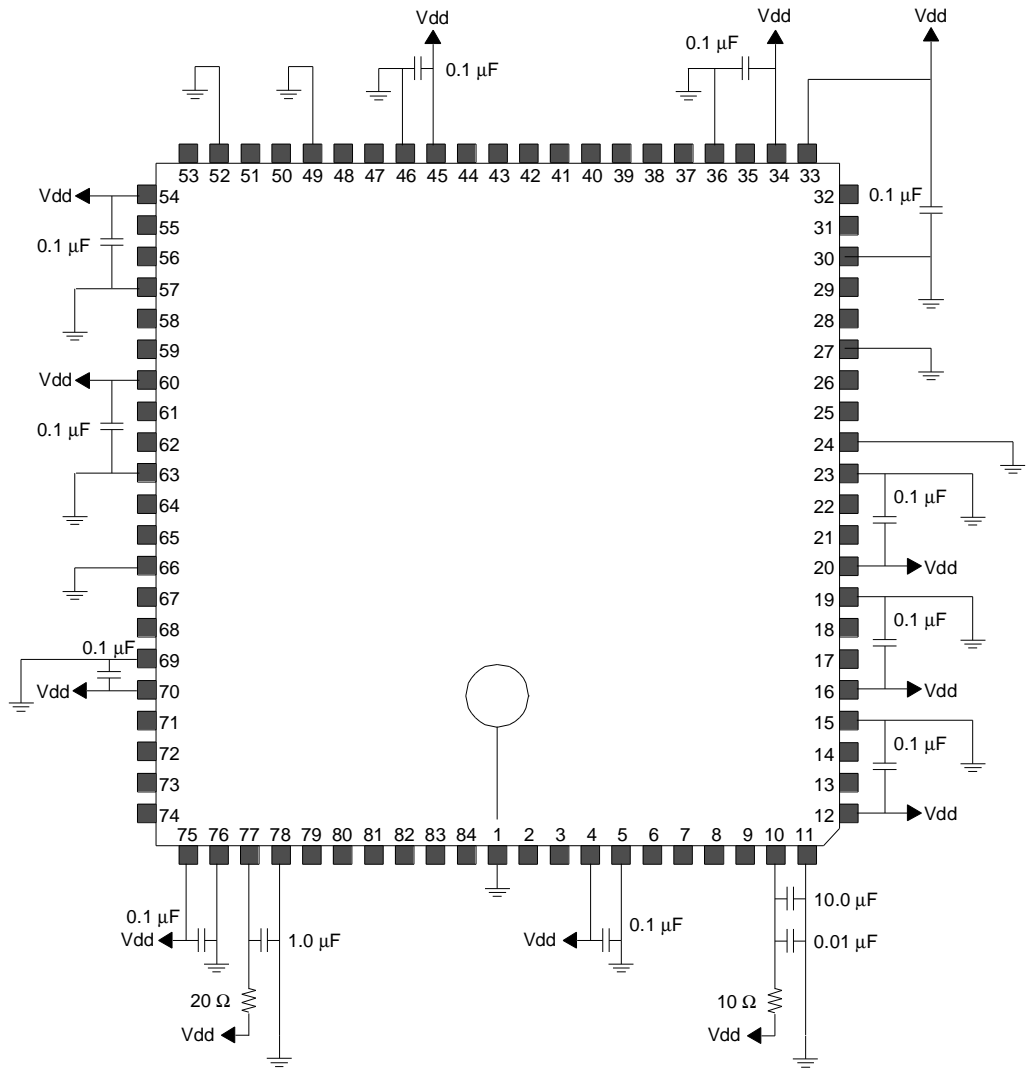
- Use the PCI reset. Because the PCI specification requires that PCI signals drive only one load, the reset should be buffered as it comes off the connector. The buffered signal can then be used to reset the 21143 and the BCM5000.
- Use an RC circuit to generate a reset pulse following power-up.
- Use a reset generator chip.
- Connect one of the general-purpose pins in the 21143 to the BCM5000 reset and apply a reset pulse to the BCM5000 through the driver.

Note: A 20-MHz or 50-MHz oscillator can be used rather than a 20-MHz crystal. When using an oscillator, the 20-pF capacitors are not required. The oscillator should be 100 ppm.

5.3.3 Power Requirements

Figure 27 shows the recommended power supply connections using the BCM5000.

Figure 27 Recommended Power Supply Connections



Note: Use solid ground and power planes.
 ← Indicates a direct connection to the power plane.
 ⊥ Indicates a direct connection to the ground plane.

5.3.4 BCM5000 Parts List

Table 27 lists the components required for this application.

Table 27 BCM5000 Application Parts List

Description	Qty	Value	Tolerance	Vendor	Part Number	Comments
10/100BASE-T4 PHY device	1	—	—	Broadcom	BCM5000 KPJ	—
Magnetics	1	—	—	Valor Pulse Engineering Fil-Mag	SF6036 PE69025 78Z-9022SM	—
RJ45-8 connector	1	—	—	—	—	—
Crystal	1	20 MHz	—	—	—	50 ppm crystal tuned to equivalent load of 15 pF ¹
Zener diode	1	2.7 V	±5%	—	—	—
LED	3	—	—	—	—	—
Diode	1	—	—	—	1N4148	—
Resistor	3	27 kΩ	±1%	—	—	RFREQ, RBIAS
Resistor	1	33 kΩ	±1%	—	—	RDAC
Resistor	1	75 kΩ	±1%	—	—	RDAC
Resistor	1	3.6 kΩ	±1%	—	—	RDAC
Resistor	1	400 Ω	±1%	—	—	—
Resistor	1	330 Ω	±1%	—	—	—
Resistor	1	20 Ω	±5%	—	—	—
Resistor	1	10 Ω	±5%	—	—	—
Capacitor	11	0.1 μF	—	—	—	—
Capacitor	1	1 μF	—	—	—	—
Capacitor	1	10 μF	—	—	—	—
Capacitor	2	20 pF	—	—	—	—

¹A 20-MHz or 50-MHz oscillator can be used rather than a 20-MHz crystal. When using an oscillator, the 20-pF capacitors are not required. The oscillator should be 100 ppm.

5.4 Layout Considerations

Consider the following issues listed in Table 28 to minimize layout problems.

Table 28 Minimizing BCM5000 Layout Problems

Component	Recommendation
Power and ground planes	Use single power and ground planes. Cut out from under the RJ45-8 and the portion of the magnetics component that interfaces to the RJ45-8.
High-frequency lines	—Keep as short as possible. —Should not be routed near or under the RDAC , FREQ or RBIAS pins.
Crystal oscillator	Place as close to the BCM5000 as possible.
Clocks and other high-frequency lines	Should not cross over the transmit and receive lines connecting the BCM5000 to the magnetics.
Bypass capacitors	Place between the power and ground planes.
Using multiple BCM5000 chips in a single application	When routing signals to the magnetics parts, avoid cross-talk between the signals.

5.5 BCM5000 Summary

This section defined the reset and power requirements, and provided recommendations on how to minimize layout problems for your design using the BCM5000.

6 NWK914 SYM PHY Network Implementation

This section describes how to interface the 21143 with the GEC Plessey Semiconductor's GPS NWK914 HuRiCAN PLUS transceiver and clock recovery device (referred to as the NWK914).

6.1 NWK914 Overview

The NWK914 was designed for three-level signaling at data rates of 100 Mb/s and 10Mb/s. The NWK914 was designed to operate at cable lengths up to 100 m (328 ft) using 100- Ω Category 5 unshielded twisted-pair UTP or 150- Ω Type 1 shielded twisted-pair STP. The NWK914 incorporates the PHY including the Medium Dependent Interface (MDI), Physical Media Attachment (PMA), and Physical Media Dependent (PMD) sublayers. It interfaces to the Physical Coding Sublayer (PCS) at the symbol level.

6.2 NWK914 Operation

For dual 10/100-Mb/s Ethernet operation, correct impedance matching must be achieved to ensure signal integrity in either 10BASE-T or 100BASE-T mode. To minimize cost, electromagnetic relays cannot be used. To overcome these constraints, the solution uses common magnetics for 10/100-Mb/s signaling with a 2:1 transmit and 1:1 receive turns ratio. Two transistors act as a differential amplifier to maintain impedance matching and for regeneration of the 10BASE-T signal. For clarity, the transmit and receive operations are described separately in the next sections for the 10-Mb/s and 100-Mb/s operations.

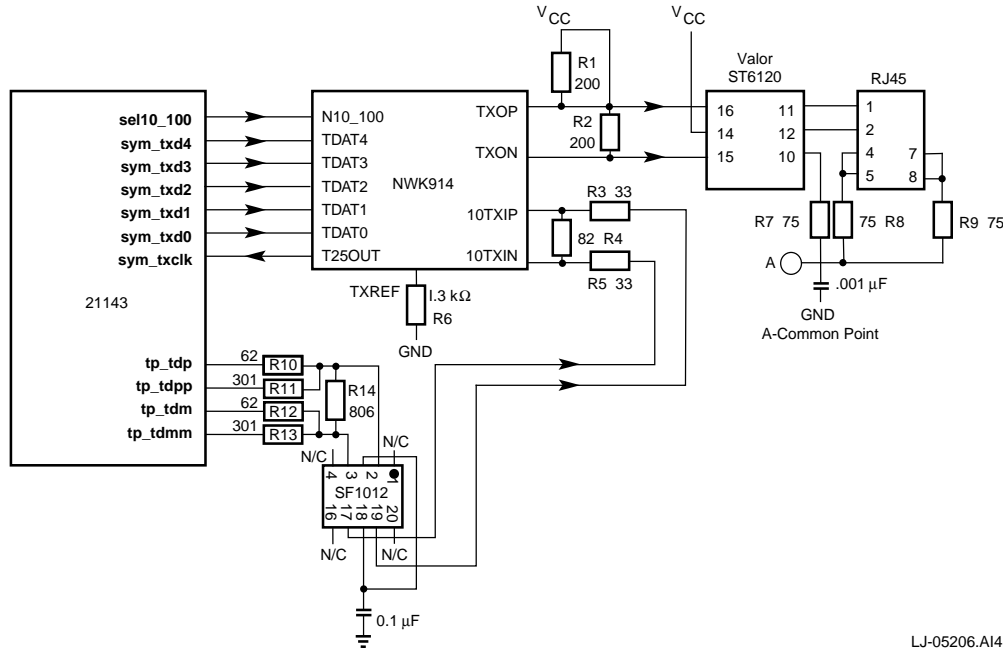
6.2.1 10-Mb/s Transmit Operation

As illustrated in Figure 28, the Digital Semiconductor **tp_tdp/m** outputs provide the standard 10BASE-T signals without any pulse shaping or filtering. The pulse shaping and filtering is provided by the resistor network (R10-R14) and the Valor SF1012 (which includes the isolation transformer and low-pass filters). The differential signal from the SF1012 is passed via the attenuation network (R3-R5) to the **10TXIP/N** inputs of the NWK914 10-Mb/s driver.

The 10BASE-T signal is then buffered and outputs to the line through the NWK914 **TXOP/N** outputs. The 400- Ω differential impedance presented to the NWK914 outputs provide an ideal termination to absorb reflections due to far-end impedance mismatch. The impedance transfer of the transformer is n^2 where n is the turns ratio. To match the 100 Ω on the cable side of the transformer, the terminating impedance needs to be 400 Ω . To ensure the correct output voltage level, the TXREF resistor is set to 1.3 k Ω (see the GEC Plessey Semiconductor Data Sheet DS4046 1.5). This produces a 10-V peak-to-peak signal on the **TXOP/N** pins of the NWK914, but this is reduced to the correct 5-V level for Ethernet signaling on the cable side of the transformer due to it being a 2:1 stepdown.

The NWK914 transmitter outputs are controlled by the **N10/100** input pin and the 21143 **sel10_100** output pin. When the **N10/100** is low, the NWK914 operates in 10-Mb/s mode. This automatically sets the correct internal current ratio for the output driver of the NWK914 when in either 10BASE-T or 100BASE-TX mode.

Figure 28 Transmit Operation



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6.2.2 100-Mb/s Transmit Operation

As illustrated in Figure 28, the 100-Mb/s mode is selected by a logic high on the **N10/100** pin of the NWK914, the signal for which is derived from the **sel10_100** pin of the 21143. In 100-Mb/s mode, the NWK914 disables the signal from the **10TXIN/P** pins thus isolating the 10-Mb/s signal path. The 100-Mb/s data is sourced directly from the 21143 via the **sym_txd0/4** pins, with the 100-Mb/s transmit signals provided on the **TXOP/N** pins of the NWK914. The differential source impedance of 400 Ω remains the same as that for 10-Mb/s operation.

6.2.3 10-Mb/s Receive Operation

Figure 29 illustrates the 10-Mb/s differential signal coupled from the cable by a 1:1 isolation transformer. The 100-Ω receive termination is achieved with the resistive network R1- R4 being 200 Ω in parallel with (R5-R8), which is also 200 Ω. The differential signals then drive the transistors Q1 and Q2 through (R5-R8). These resistors are required to ensure that the transistors Q1 and Q2 do not saturate and degrade the 10BASE-T signal quality. The transistors Q1 and Q2 are biased at $V_{cc}/2 \sim 2.5$ V via the common-mode choke of the Valor ST6120 1:1 receive transformer and the resistors R9 and R13.

The resistor R12 is selected to provide 100 mA in either collector of Q1 or Q2 to accommodate the 5-V swing required for 10BASE-T operation. It was calculated assuming that $V_{bias} = 2.5$ V, $V_{be} = 0.7$ V, and that $I_T = 100$ mA.

NWK914 Block Diagram

6.2.4 100-Mb/s Receive Operation

The 100-Mb/s signal is coupled through the same Valor ST6120 1:1 receive transformer. The 100- Ω forward cable termination is provided by the same R1-R4 and R5-R8 network. Due to the high β of Q1 and Q2, the shunt resistance is much greater than 100 Ω , and the correct cable termination is maintained.

The NWK914 **RXIP/N** input pins receive the 100-Mb/s data via the resistive network (R1-R4) to optimize the adaptive equalizer of the NWK914. For standard TP-PMD signaling, the adaptive equalizer requires a signal level of 1.12-V peak-to-peak. Given that 100BASE-TX transmission is 2-V peak-to-peak, the attenuation is approximately 56% provided by R1-R4.

The NWK914 generates a TTL signal detect output. This is asserted upon reception of a signal from the twisted-pair cable that meets the minimum amplitude specification as stated in the TP-PMD standard. The NWK914 **SDT** output is connected to the 21143 **sd** input pins. When asserted high, the **SDT** output indicates to the 21143 that the NWK914 might be receiving a valid 100BASE-TX signal.

6.3 NWK914 Block Diagram

The NWK914 interfaces with the 21143 to provide a low-cost, low-part-count solution. The block diagram in Figure 30 illustrates the GPS daughtercard design that is based upon the design outlined in Section 6.2. It interfaces directly to the 21143 motherboard via a standard 48-pin DIN connector.

The following signals are passed through the 48-pin DIN connector:

- 10-Mb/s transmit signal to the NWK914 10TX buffer
- 10-Mb/s receive data directly to the 21143
- 100-Mb/s symbol data, clock, and control signals from the 21143 to the NWK914
- 100-Mb/s signal to and from the cable can be sourced in either of the following ways:
 - a. Through the RJ45-8 on the Digital Semiconductor motherboard, through the connector, and on to the GPS daughtercard
 - b. Directly from the GPS daughtercard

Choice b optimizes 100-Mb/s performance but requires removal of the cable from the Digital Semiconductor board to the GPS board. This is considered a necessary user option because it is not desirable to have 125 Mb/s passing through a connector, which will slow data-edge speeds and potentially increase the noise level on symbol data and clocks. The RJ45-8 on the Digital Semiconductor board can be enabled or disabled with solder links (see Figure 30).

6.4.2 Layout Considerations

In order to ensure robust operation and meet an FCC compliant layout, extra considerations must be taken when designing a PCB for high-speed applications. The following parameters should be minimized:

- The distance of connecting high-speed differential data lines between components. These traces should be impedance controlled and of equal length, thus reducing ringing and delay problems.
- The number of corners. Where corners are necessary, they should be smooth and free of right angles (90°) to avoid any high-frequency aerial effects.
- Signal traces changing planes. Avoid changing signal planes to maintain a constant impedance characteristic.
- The distance the solder links are from the GPS RJ45-8. Minimize the distance to reduce signal distortion if the Digital Semiconductor RJ45-8 is unused.

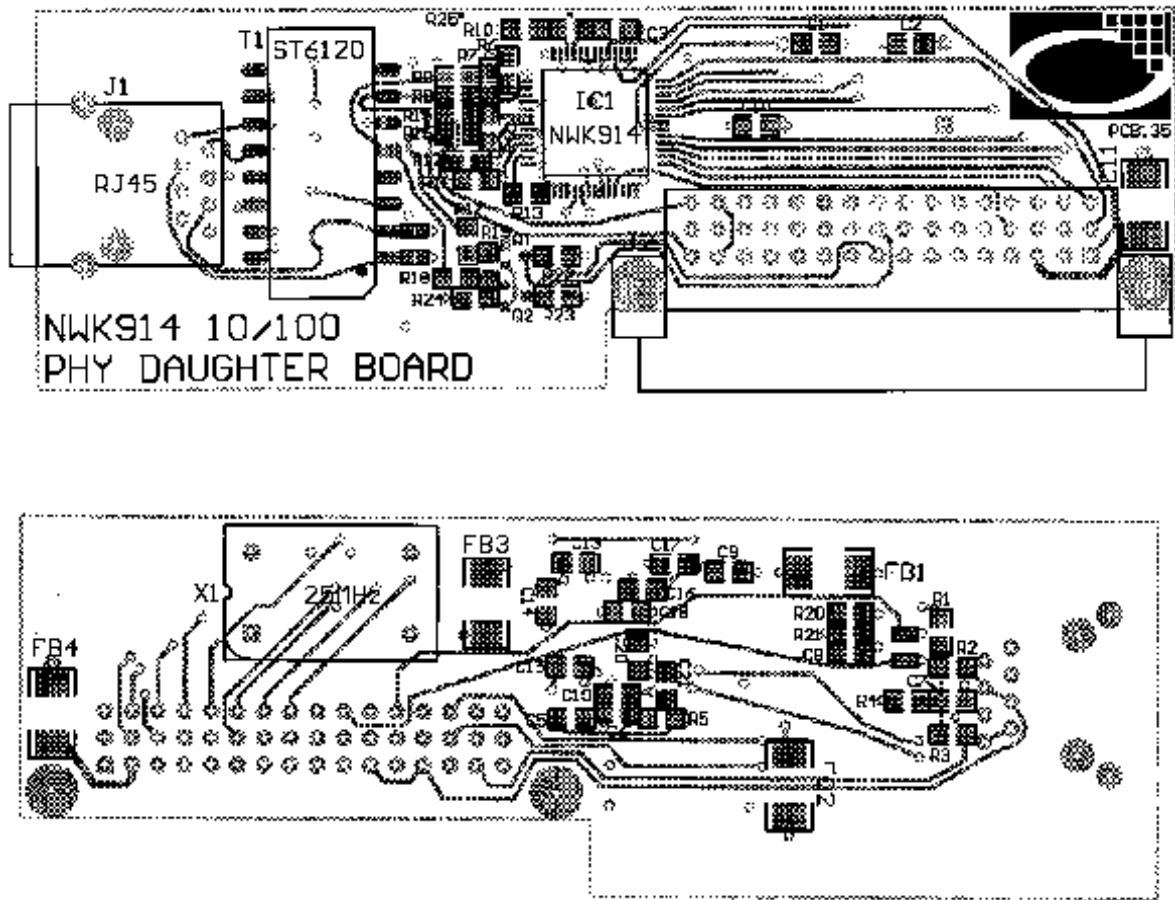
Sensitive data and clock signals should be hand routed, kept as short as possible, and kept away from clock lines (therefore, reducing noise and cross-talk).

Decoupling capacitors and the TX/RX resistors should be placed as close to the NWK914 as possible.

A shielded RJ45-8 CAT5 connector should be used to control impedances within the connector, and to prevent noise pickup. The shield should have a good electrical connection to chassis ground.

The PCB layout for the GPS daughtercard is illustrated in Figure 32.

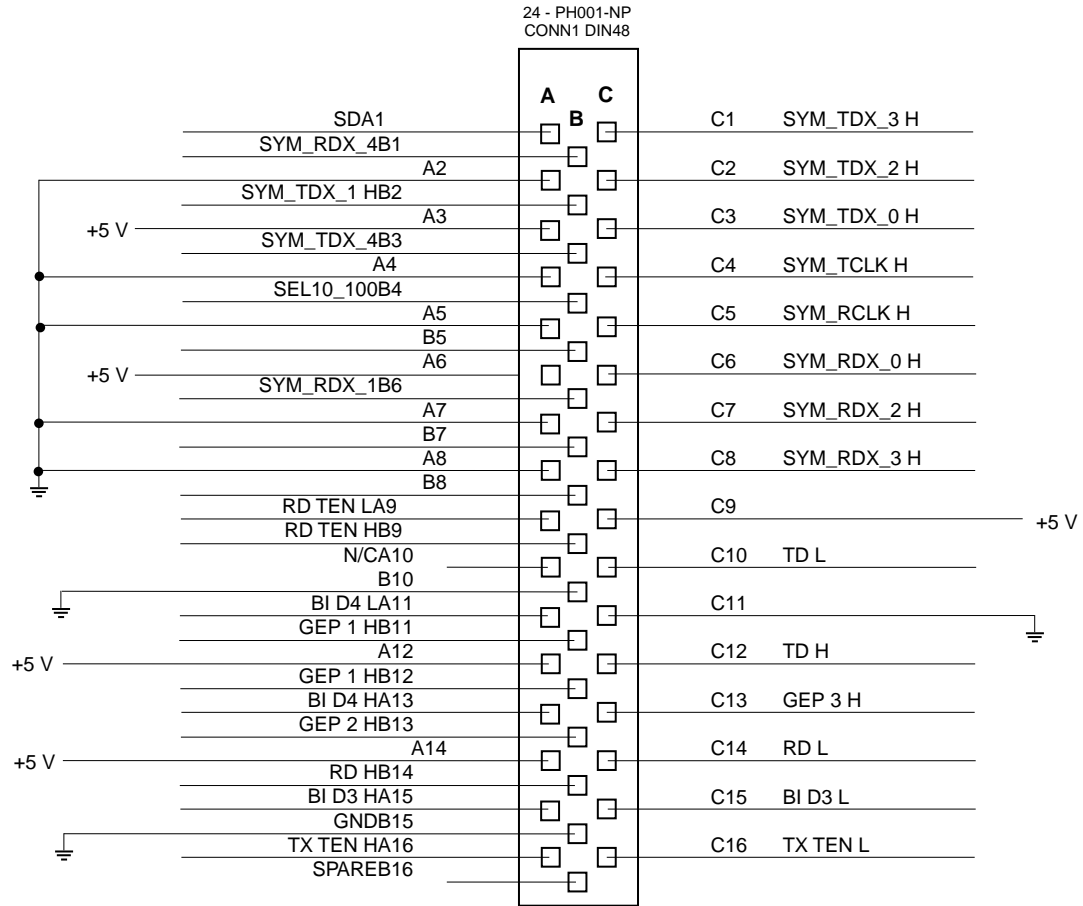
Figure 32 NWK914 10/100 PHY Daughtercard Layout



6.4.3 48-Pin DIN Connector

The specific details of the 48-pin DIN connector are illustrated in Figure 33.

Figure 33 48-Pin DIN Connector



C row is the inner row (that is, A row is the closest to the edge of the card)
 C16 is the closest pin to RJ45

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6.4.4 NWK914 Bill-of-Materials

The bill-of-materials required to build the GPS daughtercard is shown in Table 29.

Table 29 NWK914 Bill-of-Materials

(Sheet 1 of 2)

Comment	Pattern	Quantity	Component	Comment	Pattern	Quantity	Component
100n	805	2	C2, C9	2N2222A	SOT-23 SMBT2222A	2	Q1, Q2
100P	805	1	C6	33n	805	1	C5
100n	805	9	C13, C14, C15, C16, C17, C18, C19, C20, C21	33R	805	2	R15, R16
10n	805	2	C3, C8	30R	805	2	R8, R9
15P	805	1	C1	51R	805	2	R22, R23
18R	805	1	R24	68R	805	2	R6, R7
1K	805	1	R5	6.2K	805	1	R10

Power Requirements

Table 29 NWK914 Bill-of-Materials

(Sheet 2 of 2)

Comment	Pattern	Quantity	Component	Comment	Pattern	Quantity	Component
1.3k	805	1	R13	75R	805	4	R1, R2, R3, R4
1n	805	1	C7	82R	805	1	R10
200K	805	1	R25	91R	805	2	R17, R18
200R	805	4	R11, R12, R20, R21	DIN48	DIN48RA	1	J2
20R	805	1	R19	FERR	1812+	4	FB1, FB2, FB3, FB4
220n	805	1	C10	NWK914	FPQ52-0.65	1	J1
22 μ	1812+	1	C11	ST6120	'VALOR2' TRAN	1	T1
25 MHz	IQXQ-100B25.00	1	X1	—	—	—	—

6.5 Power Requirements

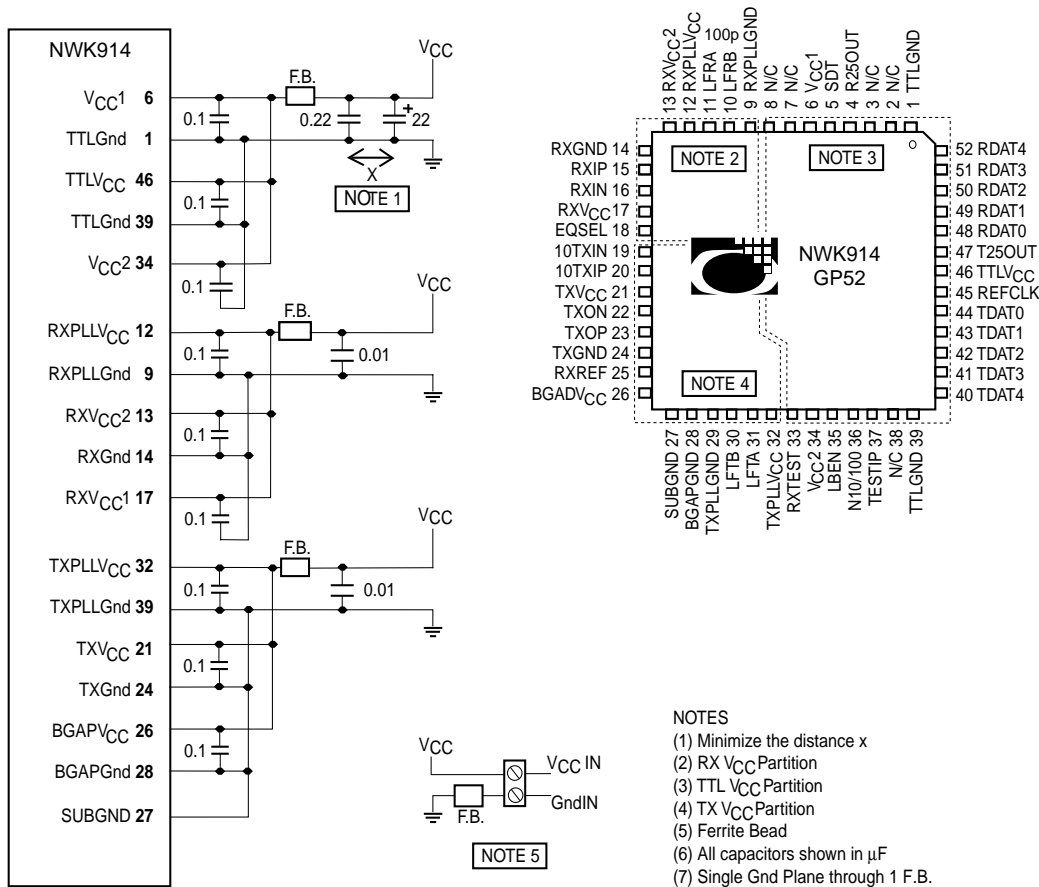
Figure 34 shows the decoupling required for the partitioning of power planes.

As shown, the TX and RX power planes should be decoupled with two chip capacitors and a ferrite bead. A continuous ground plane is practical but it can be segmented with ferrite.

The power plane should not extend in the region beyond the magnetics; this prevents noise on the plane from bypassing the common-mode filtering and coupling onto the cable. The ground plane should also not extend in the region directly underneath the magnetics.

A fully integrated design including the daughtercard and motherboard, outlined in this document, will be available as a single-board network interface card reference design.

Figure 34 Power Planes and Decoupling for the GPS PHY Daughtercard



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6.6 NWK914 Summary

This section showed how the GEC Plessey Semiconductor's NWK914 PHY device provided a cost-effective solution to the Fast Ethernet 100BASE-TX physical layer. It illustrated how to interface the Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN controller to the NWK914 to provide 10/100-Mb/s Ethernet functionality with a low part count and cost.

This design is only to confirm compatibility between the NWK914 and the 21143. The design is not intended to meet Agency Certification requirements.

For more details on the availability of the GPS NWK914 and reference design, please contact your local GEC Plessey Semiconductor Customer Service Centre.

7 QS6611 SYM PHY Network Implementation

This section describes how to interface the 21143 with the Quality Semiconductor QS6611 10/100BASE-TX transceiver (referred to as the QS6611).

7.1 QS6611 Overview

The QS6611 is a low-power CMOS 10/100BASE-TX transceiver that connects 'gluelessly' to the 21143. These two devices implement a complete 10/100 Fast Ethernet system with autonegotiation, and a combined power dissipation under 1 W. The QS6611 provides a highly integrated, low-power replacement for previous BiCMOS solutions. It is suitable for use in adapters, routers, switches, both half- and full-duplex, and repeaters/hubs including 'Class II' types. The QS6611 performs transceiver, filter, and clock functions that minimize external components and their associated noise pickup and emissions. It also includes a switchable network interface port for both 10BASE-T and 100BASE-TX operation through common magnetics, eliminating the need for dual magnetics and/or external switches or jumpers.

7.1.1 Features

The QS6611 has the following features:

- Low-power all-CMOS design; 1/3-power of BiCMOS... < 80 mA
- MLT-3 transceiver with PLL clock generation and recovery
- Category 5 UTP and Type 1 STP support
- Replacement for AM78965/6, NS83223, 10BASE-T transmit and receive filters, and 10/100 switching to magnetics
- Integrated waveshaping
- 5-bit symbol interface to PCS
- Built-in PLL loop filters to minimize external components and noise coupling
- Adaptive equalization for phase and amplitude compensation
- BASE-line wander compensation
- Built-in test modes including local and remote loopback
- Serial interface to external 10BASE-T transceiver
- Onchip filters for both 10BASE-T and 100BASE-TX
- Switched interface to common magnetics for 10/100-Mb/s modes
- Single 5-V power supply
- 64-pin QFP and TQFP surface mount packages

7.1.1.1 Features and Benefits

Table 30 outlines the QS6611 features and benefits.

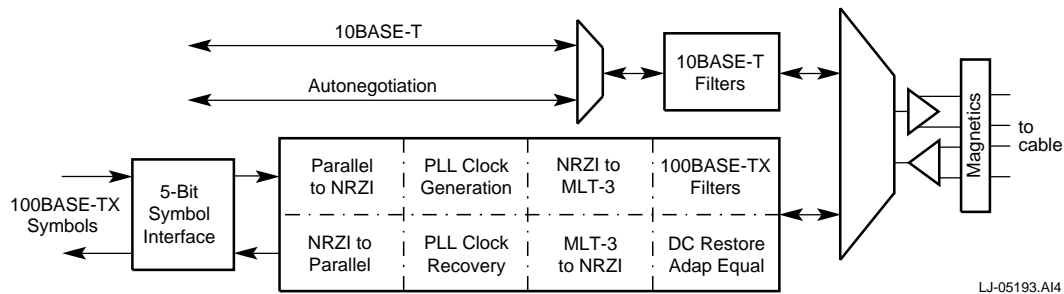
Table 30 QS6611 Features and Benefits

Features	Benefits
Fully CMOS	Low power; less than 80 mA
Adaptive equalizer	Adapts automatically to various cable lengths
QFP and VQFP (thin) packs	PCI/CardBus/hubs/switcher
10BASE-T transmit filters	No external hybrid L-C filters
10/100 multiplexing	No external relay or switchers
Crystal-ready 125/20-MHz clock synthesis	1/3-cost of oscillator module
Digital clock recovery PLL with integrated loop filters	No external loop filter components required

7.2 QS6611 System Diagram

Figure 35 shows the system diagram for the QS6611.

Figure 35 QS6611 System Diagram



7.3 QS6611 Schematic

This section describes how to connect the QS6611 to the network and to the 21143, and provides layout considerations.

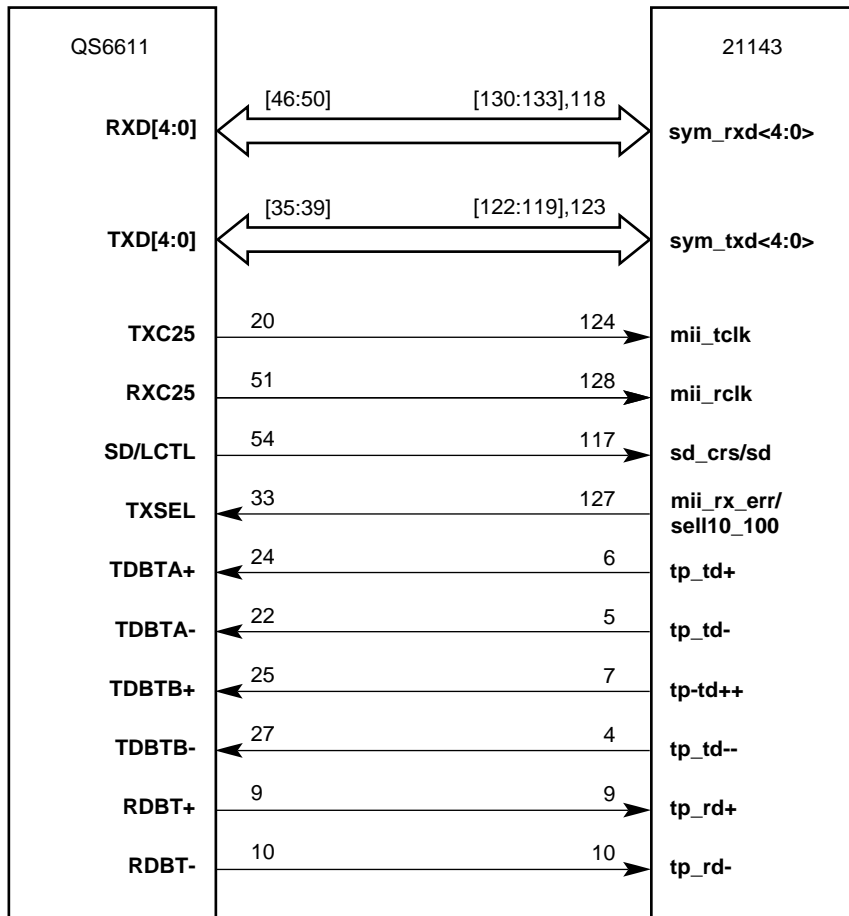
7.3.1 Network Connections

Figure 36 shows how to connect the QS6611 to the network.

7.3.2 21143 Connections

Figure 37 shows how to connect the QS6611 to the 21143.

Figure 37 Connecting the QS6611 to the 21143



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7.3.3 Layout Considerations

Consider the following recommendations in Table 31 for the PWB layout of the QS6611 and 21143 in a PCI adapter.

Table 31 QS6611 PWB Layout Recommendations

(Sheet 1 of 2)

Recommendation	Comments
<p>Refer to Figure 38 for recommended parts positioning. Place the QS6611, the transformer module, and the RJ45 connector as close to each other as possible for best transmission and least noise pickup and emissions.</p>	<p>The area under the RJ45 connector and the near edge of the magnetics module (under the pins) should be isolated from the Vcc and ground planes, and should have its own “chassis ground” plane as shown in Figure 38.</p>
<p>Do not segment the Vcc power plane or ground plane. Use a single, continuous plane for Vcc and ground to which all power pins (Vcc and Gnd) will connect through vias as close to the pins as possible.</p>	<p>Splitting the Vcc power supply plane into segments for different Vcc pins on the QS6611 is not needed, and may cause problems in bypassing the various segments.</p>
<p>Refer to Figure 36 for recommended pin connections.</p>	<p>Certain unused pins on the QS6611 need to be tied high or low as shown in Figure 36.</p>
<p>For best results, use a crystal, rather than a clock oscillator. Place the crystal as close to the X1 and X2 pins (pins 21 and 22) as possible, and keep traces short and direct.</p>	<p>Use 25 MHz $\pm 0.005\%$, CL = 39 pF, AT Cut, Parallel Resonant (for example, ECS250.18).</p>
<p>Place the 4.99-kΩ, 1%, 1/8-W current reference resistor as close to the IREF pin (pin 6) as possible.</p>	<p>See Figure 38.</p>
<p>Keep transmit and receive pair runs as short as possible. Keep the separation between the two conductors of each pair fairly wide, 1 or 1.5 mm if possible, using the same separation width all along the run to improve transmission characteristics. Keep the separation between adjacent pairs on the same layer (or adjacent layers not separated by a power or ground plane) wide, 2 mm or more if possible, to minimize cross-talk.</p>	<p>Transmit and receive pairs should not cross over each other. They should not be laid one on top of the other on adjacent planes (but this is allowed if a power or ground plane is placed between the other planes). The two traces of a pair should never cross over each other.</p>
<p>Keep high-frequency traces short, and space them apart from each other and from traces that may be sensitive, to improve transmission and reduce cross-talk. Especially sensitive are clock lines, high-speed bus lines, high-impedance lines (passively-driven lines), analog lines, and the symbol interface lines.</p>	<p>Where long, high-speed lines cannot be avoided, ringing and echo problems can be treated with series resistors at the source end and termination resistors to ground or Vcc at the far ends.</p>

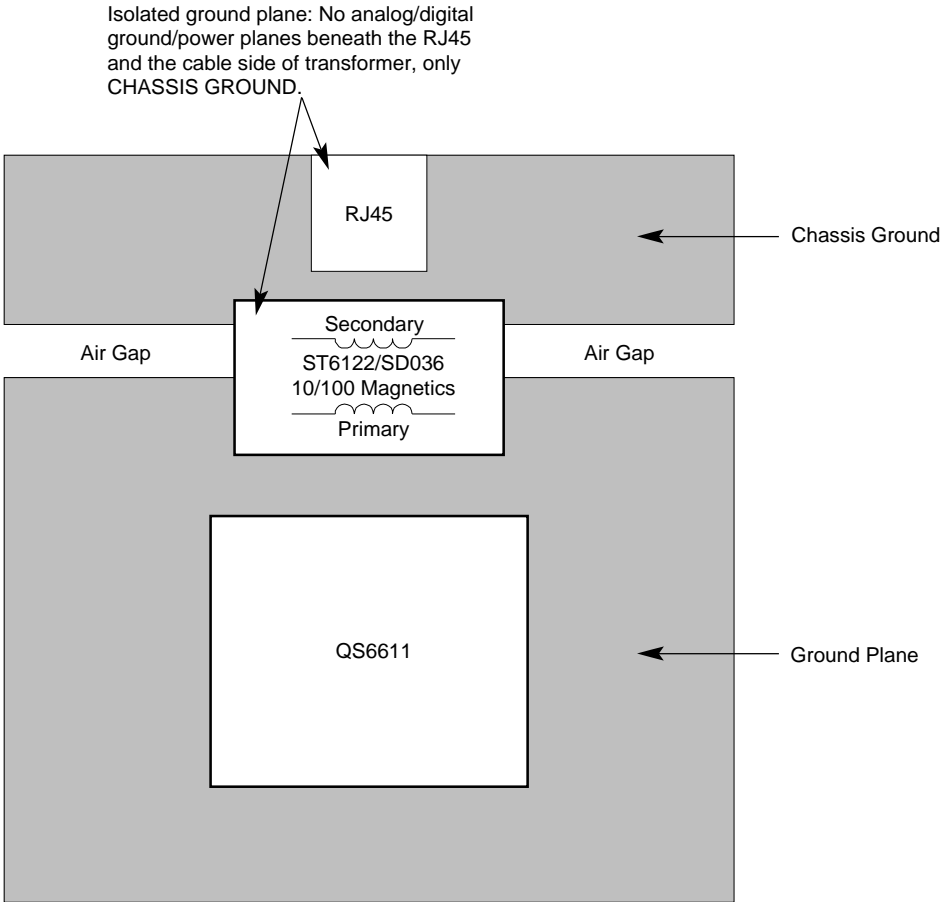
Table 31 QS6611 PWB Layout Recommendations (Sheet 2 of 2)

Recommendation	Comments
Never route clock or high-speed signal lines immediately under the body of the QS6611 chip.	If there is a ground or power plane shielding the QS6611, it is allowed.
Layout pads for the 230-Ω resistor and 0.1-μF capacitor on pin 26, and minimum length traces as shown in Figure 39.	Later revision of the QS6611 will probably not need this resistor. The recommended layout allows omission of this resistor without PCB layout change.
Use two 1000-pF capacitors in the RDBT± line (pins 9 and 10) to decouple the dc common-mode voltage between the Digital Semiconductor 21143 and the QS6611.	See Figure 36.

7.3.4 Ground-Plane Partitioning

As shown in Figure 38, isolating circuits on the primary side from the secondary side of the transformer with an air gap can reduce noise.

Figure 38 PWB Noise Reduction

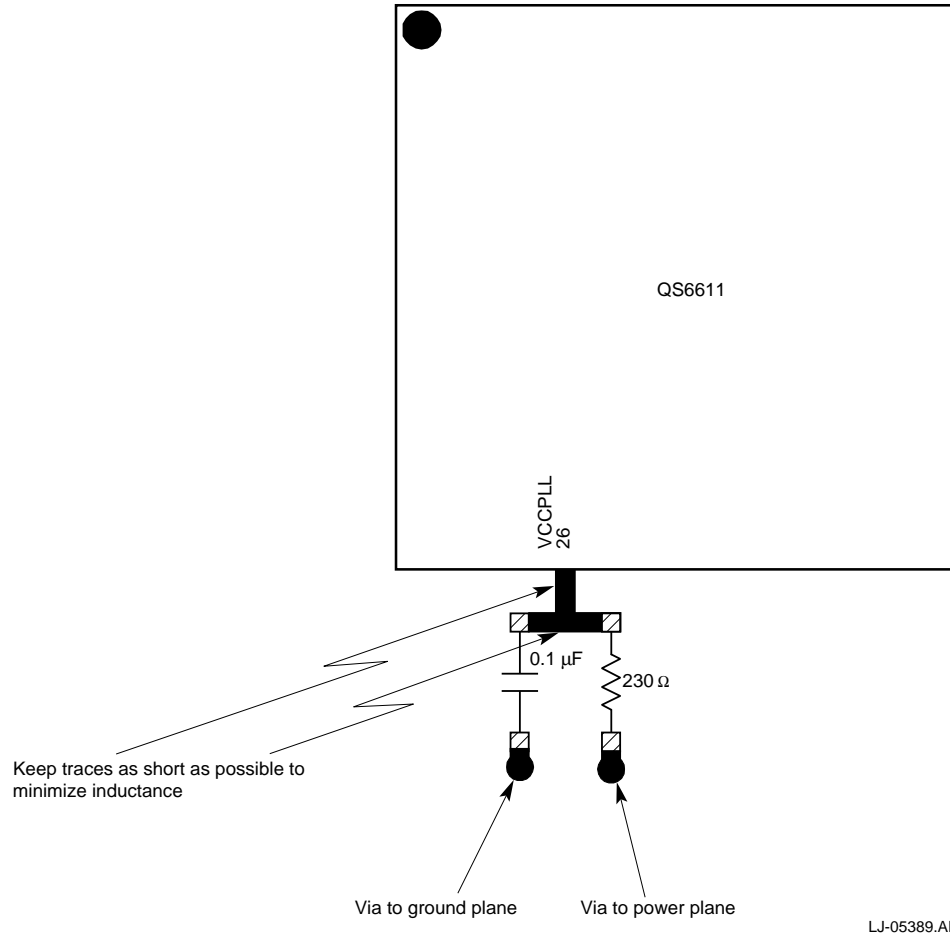


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7.3.5 VCCPLL Connections

Figure 39 shows how to connect the VCCPLL pin on the QS6611.

Figure 39 Connecting the VCCPLL on the QS6611



7.4 QS6611 Summary

This section provided information on how to connect the QS6611 to the 21143. Layout considerations and ground-plane partitioning to reduce signal noise were also provided.

A National Semiconductor License Agreement

Common Magnetics License Agreement

Dear Customer:

The attached application notes describe a common magnetics implementation of a 10/100 Ethernet physical layer and transceiver using National Semiconductor Corporation's DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and DP83223V TWISTER™ High Speed Networking Transceiver Device.

The following suppliers have indicated that they intend to provide magnetic components for the National Semiconductor Corporation recommended implementation. This is not an exclusive list and National Semiconductor makes no warranty as to the suitability of any of the magnetics suppliers listed:

Bel Fuse
Fil-Mag Technical
HALO Electronics
Kappa Technology
Nano Pulse
PCA
Pulse Engineering
Valor Electronics
TDK

The above referenced companies' product(s) in conjunction with National Semiconductor Corporation's part number DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and National Semiconductor Corporation's part number DP83223V may be designed as a common magnetics front end for a 10/100 Mb/s Ethernet system. A system utilizing this common magnetics arrangement is intended to provide combination 10BASE-T and 100BASE-T capabilities.

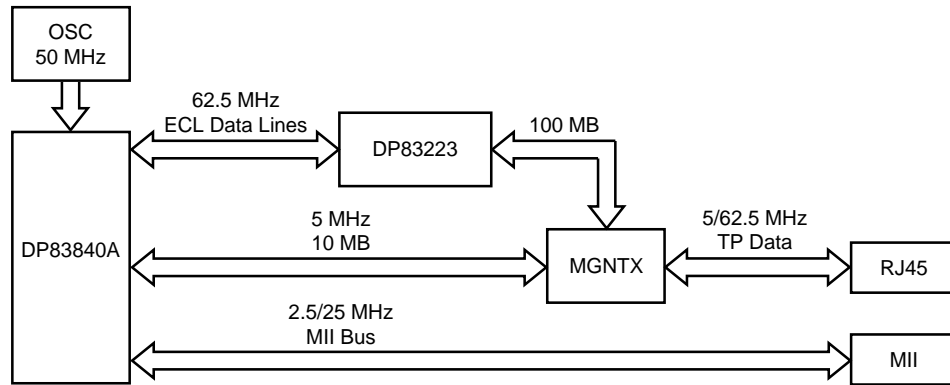
National Semiconductor Corporation's part number DP83223V is covered by U.S. Patent Nos. 5,337,025 and 5,444,410, and the system and methods of operation of the common magnetics arrangement are covered by one or more pending patents of National Semiconductor Corporation. National Semiconductor Corporation offers a non-transferable license under the patents, which license is subject to royalties to be agreed on between National Semiconductor Corporation and the customer. National Semiconductor hereby also grants purchasers of both National Semiconductor Corporation's DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and DP83223V components a non-exclusive, paid-up, non-transferable license under such pending patents and those patents which issue therefrom, to make, use and sell such systems **which utilize both of National Semiconductor Corporation's DP83840AVCE 10/100 Mb/s Ethernet Physical Layer and DP83223V components.**

National Semiconductor Physical Layer Design Recommendations

The following schematics represent the National Semiconductor 10/100 Ethernet Physical Layer design recommendations. This implementation might vary from the Digital Semiconductor Reference Design, due to the designer's preferences, and might differ from any other given application implementation as well. Again these recommendations are intended to improve the designer's understanding of Fast Ethernet systems, and with that understanding, a designer is able to develop systems more effectively.

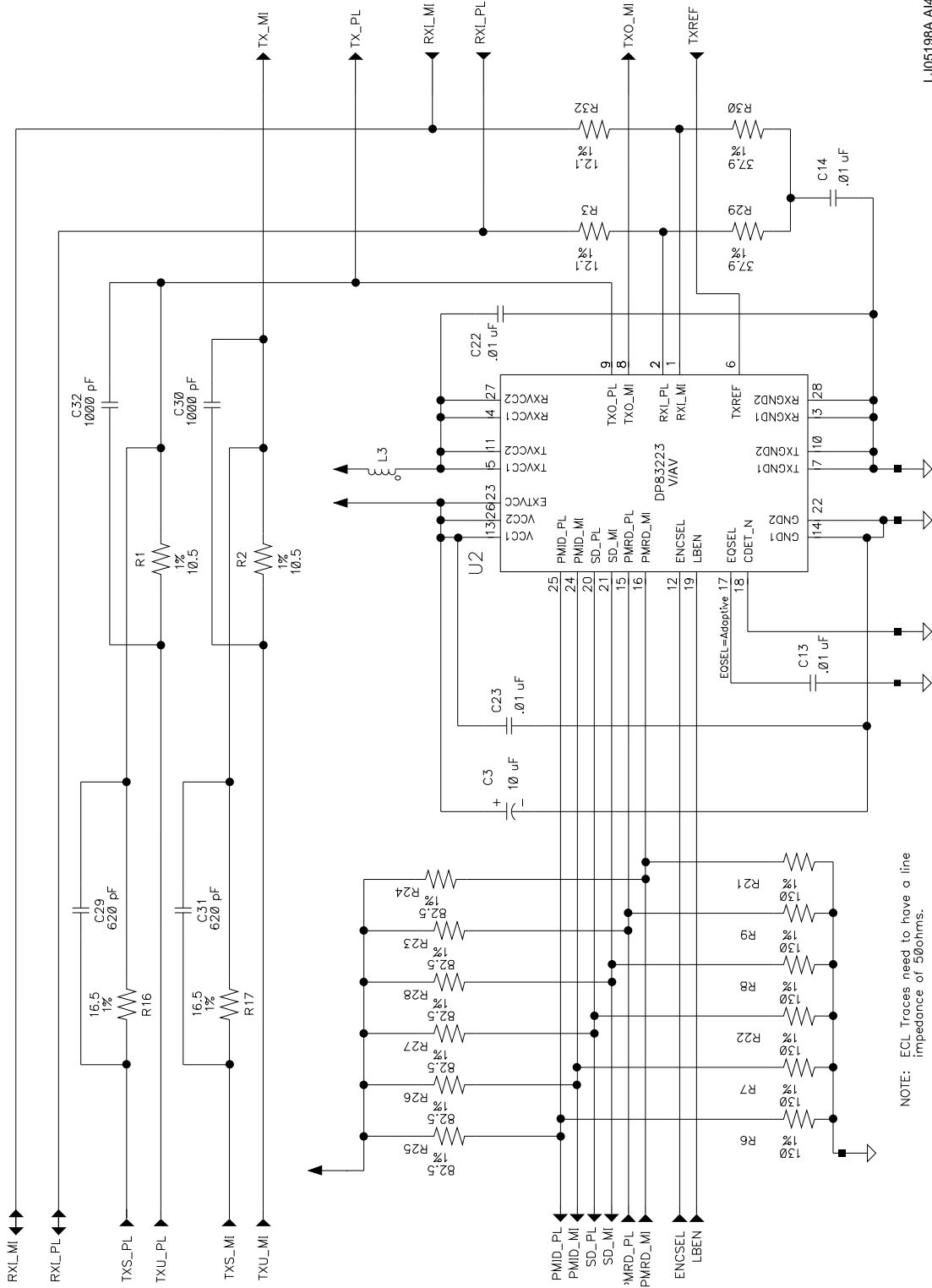
Note: The value of C8 should be 820 pF instead of 1000 pF as shown in Figure 43.

Figure 40 10/100 Ethernet Physical Layer Block Diagram



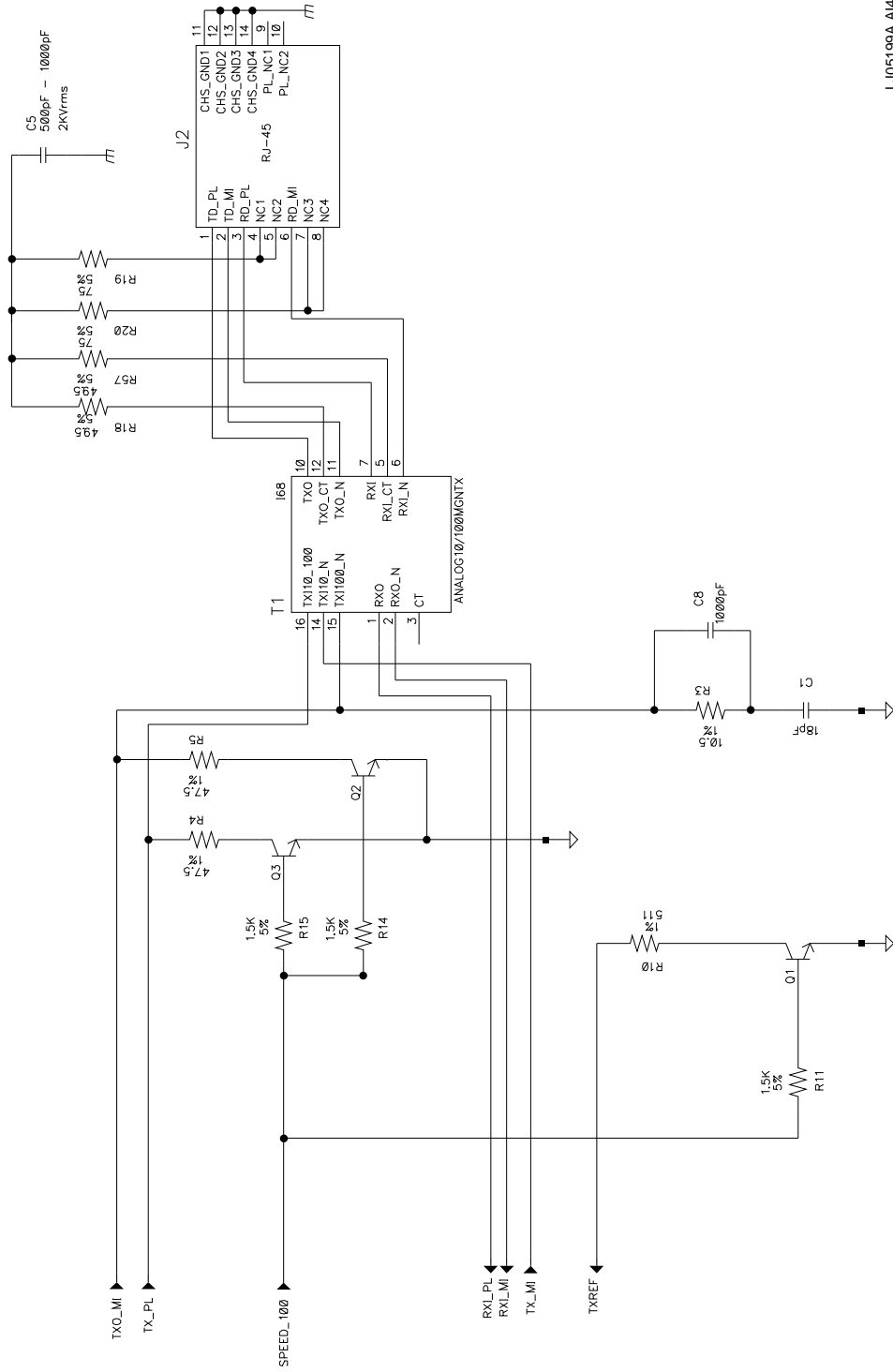
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Figure 42 DP83223V



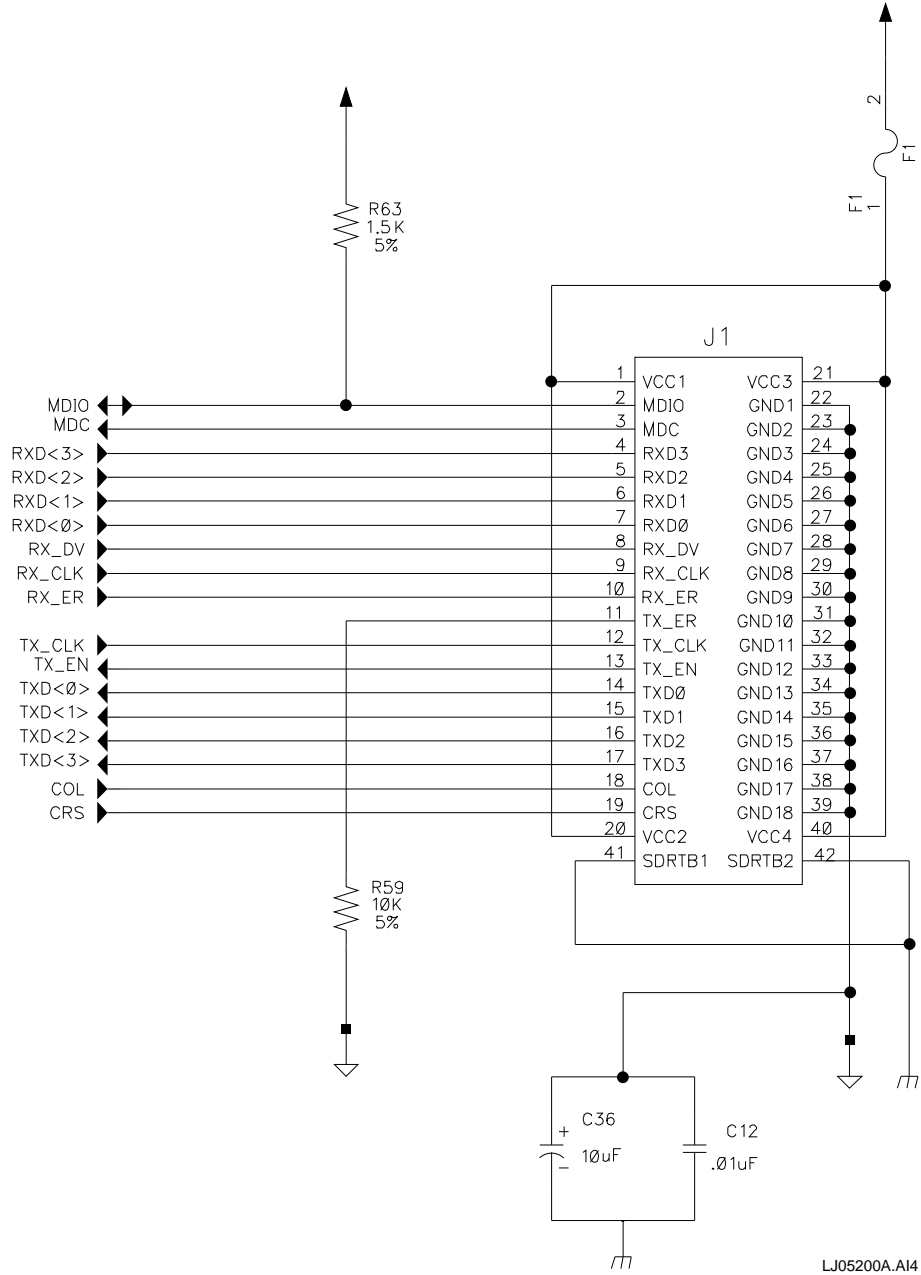
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Figure 43 Twisted Pair



LJ05199A.A14

Figure 44 MII Interface



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World Wide Web Internet site <http://www.digital.com/info/semiconductor>
United States and Canada **1-800-332-2717**
Outside North America **+1-508-628-4760**

Ordering Digital Semiconductor Products

To order the Digital Semiconductor 21143 PCI/CardBus Fast Ethernet LAN Controller and for more information about an evaluation board kit, contact your local distributor. To obtain a *Digital Semiconductor Product Catalog*, call the Digital Semiconductor Information Line.

The following table lists some of the semiconductor products available from Digital Semiconductor:

Product	Order Number
Digital Semiconductor 21143 PCI 10/100BASE-TX Evaluation Board Kit	21A43-01
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (PQFP package)	21143-PA
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (TQFP package)	21143-TA

Ordering Associated Digital Semiconductor Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, call the Digital Semiconductor Information Line or visit Digital Semiconductor's World Wide Web Internet site.

Title	Order Number
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Product Brief	EC-QW2CA-TE
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Data Sheet	EC-QWC3A-TE
Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual	EC-QWC4A-TE
Digital Semiconductor 21143 10/100 BASE-TX Evaluation Board User's Guide	EC-QXZSA-TE

Obtaining Third-Party Technical Support or Products

If you need third-party technical support or products, call the related vendor.

Broadcom Corporation

If you need Broadcom technical support, products, or help deciding which Broadcom literature best meets your needs, call **1-714-450-8700**.

The following table lists some of the products available from Broadcom:

Product	Order Number
BCM5000 10/100BASE-T4 Fast- Φ chip (84-pin PLCC package)	BCM5000 KPJ
BCM5000 10/100BASE-T4 Fast- Φ chip (100-pin PQFP)	BCM5000 KPF
BCM5000 10/100BASE-T4 Fast- Φ Transceiver Data Sheet	—
Application note for BCM5000 10/100BASE-T4 Fast- Φ Transceiver	—
Schematic set for the BCM5000 PCI 100BASE-T4 Adapter based on the 21140A	—

GEC Plessey Semiconductors

If you need GEC Plessey Semiconductors technical support, products, or help deciding which GEC Plessey Semiconductors literature best meets your needs, call:

- **(01793) 518000** (United Kingdom)
- **1-408-438-2900** (United States of America)

The following table lists some of the products available from GEC Plessey Semiconductors:

Product	Order Number
NWK914 HuRiCAN PLUS transceiver and clock recovery device	—
DS4046 1.5 (Data Sheet)	DS4046 1.5

ICS

If you need ICS technical support, products, or help deciding which ICS literature best meets your needs, contact one of the following persons:

- Fred Jones **610-630-5259** (U.S. East and Europe regions)
- Greg McClenon **408-291-2541** (U.S. Central and West regions)
- John Sundell **408-271-2527** (U.S. West and Pacific Rim regions)

Additional information can be obtained from ICS's World Wide Web Internet site:

<http://www.icsinc.com>.

The following table lists some of the products available from ICS:

Product	Order Number
ICS1890 10BASE-T/100BASE-TX Integrated PHYceiver (PQFP Package)	ICS1890Y
ICS1890 10BASE-T/100BASE-TX Integrated PHYceiver (TQFP Package)	ICS1890Y-14

Micro Linear

If you need Micro Linear technical support, products, or help deciding which Micro Linear literature best meets your needs, call **1-408-433-5200** extension **403**.

Data sheets and application notes can be obtained by calling Micro Linear at the above number, by sending an e-mail to **info@ulinear.com**, or by downloading them from Micro Linear's World Wide Web Internet site:

<http://www.microlinear.com>.

The following table lists some of the products available from Micro Linear:

Product	Order Number
ML6692 100BASE-TX PHY device	—

National Semiconductor

If you need National Semiconductor technical support, products, or help deciding which National Semiconductor literature best meets your needs, call **1-800-272-9959**.

The following table lists some of the products available from National Semiconductor:

Product	Order Number
DP83223V Transceiver product samples	—
DP83840A Physical Layer product samples	—
10/100 Ethernet Common Magnetics application note	—
10/100 BASE-T Magnetics Specification	—
1996 National Ethernet Databook	—
DP83223A Transceiver data sheets	—
DP83223 TWISTER Adaptive Equalization Considerations application note	—
DP83840A Proprietary User Informations	—
DP83840A Physical Layer data sheets	—
National Semiconductor Fast Ethernet Physical Layer Design Kit	—
Transmission Line Concepts and System Considerations application note	—
Unmanaged Repeater application note	—

QSI

If you need QSI technical support, products, or help deciding which QSI literature best meets your needs, call **1-408-450-8080**.

The following table lists some of the products available from QSI:

Product	Order Number
QS6611 10/100BASE-TX transceiver	—

Ordering PCI and IEEE Literature

You can order the following PCI and IEEE literature directly from the vendor:

Title	Vendor
<i>PCI Local Bus Specification, Revision 2.1</i>	PCI Special Interest Group
<i>PCI Multimedia Design Guide, Revision 1.0</i>	U.S. 1-800-433-5177
<i>PCI System Design Guide</i>	International 1-503-797-4207
PCI-to-PCI Bridge Architecture Specification, Revision 1.0	FAX 1-503-234-6762
PCI BIOS Specification, Revision 2.1	
IEEE standards 802.3, 802.3u, and 1149.1	The Institute of Electrical and Electronics Engineers, Inc.
	U.S. 1-800-701-4333
	International 1-908-981-0060
	FAX 1-908-981-9667